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Cascaded Two-Level Inverter-Based Multilevel STATCOM for High-Power Applications

D.Rajesh Naik
M.Tech-Power Electronics,
Department of EEE,
SRTIST Nalgonda, Telangana.

E.Ravi Naik
Assistant Professor,
Department of EEE,
SRTIST Nalgonda, Telangana.

ABSTRACT:

In this paper, a simple static var compensating scheme using a cascaded two-level inverter-based multilevel inverter is proposed. The topology consists of two standard two-level inverters connected in cascade through open-end windings of a three-phase transformer. The dc-link voltages of the inverters are regulated at different levels to obtain four-level operation. The simulation study is carried out in MATLAB/SIMULINK to predict the performance of the proposed scheme under balanced and unbalanced supply-voltage conditions. A laboratory prototype is developed to validate the simulation results. The control scheme is implemented using the TMS320F28335 digital signal processor. Further, stability behavior of the topology is investigated. The dynamic model is developed and transfer functions are derived. The system behavior is analyzed for various operating conditions.

INTRODUCTION:

The application of flexible ac transmission systems (FACTS) controllers, such as static compensator (STATCOM) and static synchronous series compensator (SSSC), is increasing in power systems. This is due to their ability to stabilize the transmission systems and to improve power quality (PQ) in distribution systems. STATCOM is popularly accepted as a reliable reactive power controller replacing conventional var compensators, such as the thyristor-switched capacitor (TSC) and thyristor-controlled reactor (TCR). This device provides reactive power compensation, active power oscillation damping, flicker attenuation, voltage regulation, etc. Generally, in high-power applications, var compensation is achieved using multilevel inverters. These nverters consist of a large number of dc sources which are usually realized by capacitors. Hence, the converters draw a small amount of active power to maintain dc voltage of capacitors and to compensate the losses in the converter. However, due to mismatch in conduction and switching losses of the switching devices, the capacitors voltages are unbalanced. Balancing these voltages is a major research challenge in multilevel inverters. Various control schemes using different topologies are reported in. Among the three conventional multilevel inverter topologies, cascade H-bridge is the most popular for static var compensation. However, the aforementioned topology requires a large number of dc capacitors. The control of individual dc-link voltage of the capacitors is difficult. Static var compensation by cascading conventional multilevel/ two level inverters is an attractive solution for high-power applications. The topology consists of standard multilevel/twolevel inverters connected in cascade through open-end windings of a three-phase transformer. Such topologies are popular in high-power drive. One of the advantages of this topology is that by maintaining asymmetric voltages at the dc links of the inverters, the number of levels in the output voltage waveform can be increased.

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This improves PQ. Therefore, overall control is simple compared to conventional multilevel inverters. Various var compensation schemes based on this topology are reported in In, a three-level inverter and twolevel inverter are connected on either side of the transformer low-voltage winding. The dc-link voltages are maintained by separate converters. In, three-level operation is obtained by using standard two-level inverters. The dc-link voltage balance between the inverters is affected by the reactive power supplied to the grid. In this paper, a static var compensation scheme is proposed for a cascaded two-level inverter-based multilevel inverter. The topology uses standard two-level inverters to achieve multilevel operation. The dc-link voltages of the inverters are regulated at asymmetrical levels to obtain four-level operation. To verify the efficacy of the proposed control strategy, the simulation study is carried out for balanced and unbalanced supply-voltage conditions. A laboratory prototype is also developed to validate the simulation results.

From the detailed simulation and experimentation by the authors, it is found that the dc-link voltages of two inverters collapse for certain operating conditions when there is a sudden change in reference current. In order to investigate the behavior of the converter, the complete dynamic model of the system is developed from the equivalent circuit. The model is linearized and transfer functions are derived. Using the transfer functions, system behavior is analyzed for different operating conditions.This paper is organized as follows: The proposed control scheme is presented in Section II. Stability analysis of the converter is discussed in Section III. Simulation and experimental results are presented in Sections IV and V, respectively.

Control Strategy

The control block diagram is shown in Fig. 1. The unit signals coswt and sin wt are generated from the phase-locked loop (PLL) using three-phase supply voltages(va,vb,vc).

The converter currents(ia,ib,ic) are transformed to the synchronous rotating reference frame using the unit signals. The switching frequency ripple in the converter current components is eliminated using a low-pass filter (LPF).

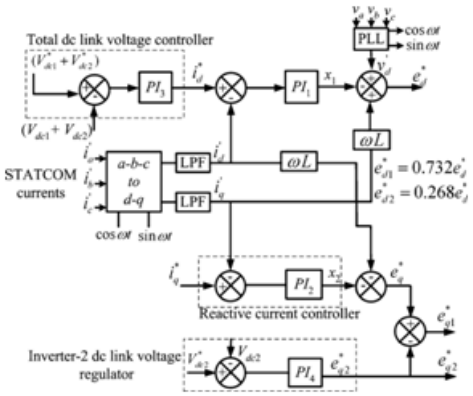

Fig. 1. Control block diagram.

EXPERIMENTAL RESULTS

The system configuration shown in Fig. 1 is considered for simulation. The simulation study is carried out usingMATLAB/ SIMULINK. The system parameters are given in Table I.

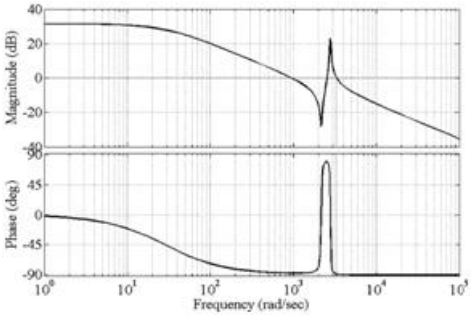

Fig. 2

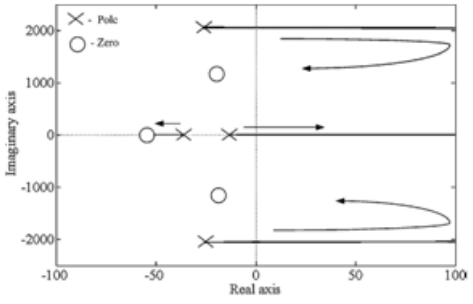

Fig 3.

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TABLE I: Simulation System Parameters

Rated power	5 MVA
Transformer voltage rating	11kV/400
AC supply frequency, f	50 Hz
Inverter-1 dc link voltage, V_{dc1}	659 V
Inverter-2 dc link voltage, V_{dc2}	241 V
Transformer leakage reactance, X_l	15%
Transformer resistance, R	3%
DC link capacitances, C_1, C_2	50 mF
Switching frequency	1200 Hz

A. Reactive Power Control

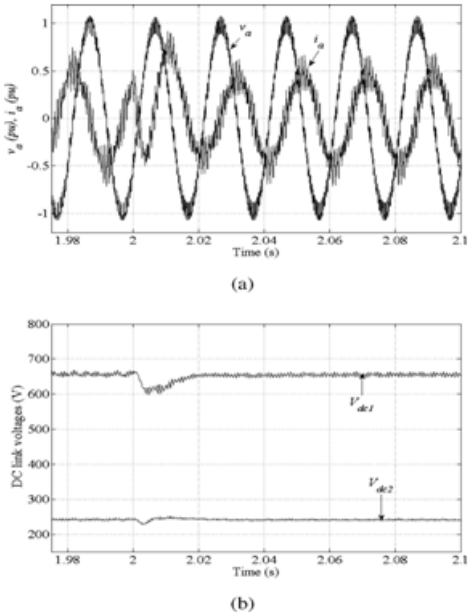

Fig. 4.Reactive power control. (a) Source voltage and inverter current. (b) DC-link voltages of two inverters.

B. Load Compensation

In this case, the STATCOM compensates the reactive power of the load. Initially, STATCOM is supplying a current of 0.5p.u. At t=2.0 s, the load current is increased so that STATCOM supplies its rated current of 1 p.u. Fig. 5(a) shows source voltage and converter current, while Fig. 5(b) shows the dc-link voltages of two inverters. The dc-link voltages are maintained at their respective reference values when the operating conditions are changed.

C. Operation During the Fault Condition

In this case, a single-phase-to-ground fault is created at1.2 s, on the phase of the HV side of the 33/11-kVtransformer.The fault is cleared after 200 ms. voltages across the LV side of the 33/11-kV transformer. Fig. the - axes components of negative-sequence current of the converter. These currents are regulated at zero during the fault condition. A scaled down laboratory prototype is developed for the validation of the proposed var compensation scheme. The experimental setup consists of two insulated-gate bipolar transistor (IGBT)-based two-level inverters connected in cascade on the LV side of the 6-kVA, 200/400-V, three-phase transformer. The

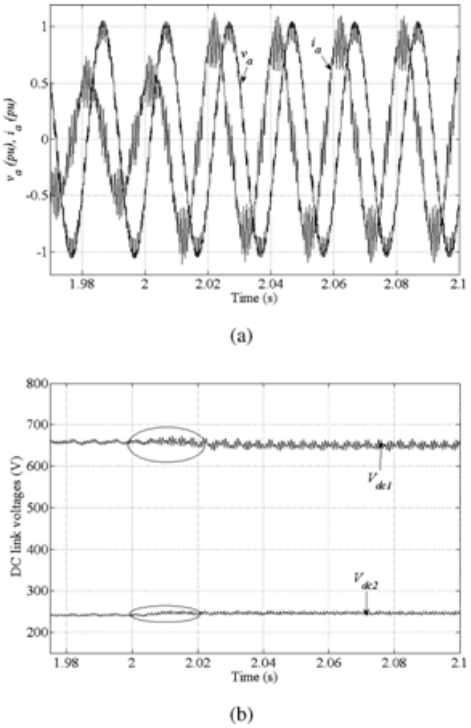

Fig. 5. Load compensation. (a) Source voltage and inverter current. (b) DC-link voltages of two inverters.

HV side of the transformer is connected to supply lines. The transformer has resistance and leakage reactance of 5.1% and 3.6%, respectively. The control strategy is implemented using TMS320F28335. The switching frequency is set at 1.2 kHz.

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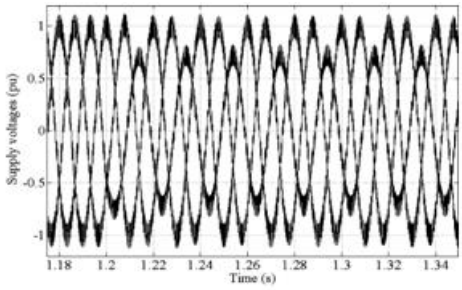
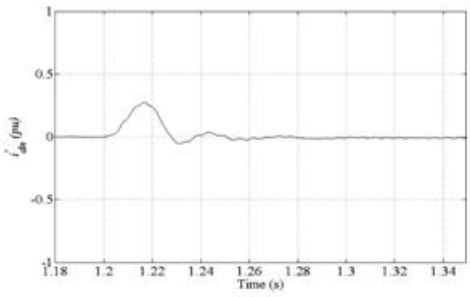
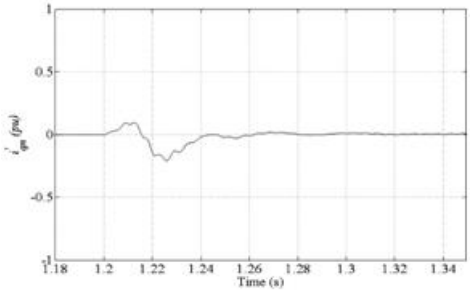
The dc-link voltages of inverters 1 and 2 are regulated at 88 V and 32 V, respectively. The source voltage is kept at 70 V(rms). The reactive power is directly injected into the source by keeping the reference current at a particular value.



(a)



(b)



(c)

CONCLUSION:

DC-link voltage balance is one of the major issues in cascaded inverter-based STATCOMs. In this paper, a simple var Fig. 10. Experimental result: Capacitive mode of operation. (a) Source voltage (50 V/div) and STATCOM current (5 A/div). (b) DC-link voltages of inverter-1 and inverter-2 (20 V/div). Time scale: 5 ms/div. (c) Harmonic spectrum of current. compensating scheme is proposed for a cascaded two-level inverter- based multilevel inverter.

The scheme ensures regulation of dc-link voltages of inverters at asymmetrical levels and reactive power compensation. The performance of the scheme is validated by simulation and experimentations under balanced and unbalanced voltage conditions. Further, the cause for instability when there is a change in reference current is investigated. The dynamic model is developed and transfer functions are derived. System behavior is analyzed for various operating conditions. From the analysis, it is inferred that the system is a non minimum phase type, that is, poles of the transfer function always lie on the left half of the - plane. However, zeros shift to the right half of the - plane for certain operating conditions. For such a system, oscillatory instability for high controller gains exists.

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