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# Logical reversibility of computation Using Reversible Complex Multipliers

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***ABSTRACT:***
***Reversible logic is an important area to carry the computation into the world of quantum computing. In this paper a 4-bit multiplier using a new reversible logic gate called BVPPG gate is presented. BVPPG gate is a 5 x 5 reversible gate which is designed to generate partial products required to perform multiplication and also duplication of operand bits is obtained. This reduces the total cost of the circuit. Toffoli gate is the universal and also most flexible reversible logic gate. So we have used the Toffoli gates to construct the designed multiplier.***

***KEYWORDS:*** ***Reversible logic gates, Toffoli gates, partial products, multiplier, quantum computing, Nanotechnology, Fu-ture computing.***

## 1. INTRODUCTION:

In 1961, Rolf Landauer [2] in his principle stated that the heat coming from computation was due to the destruction of information (wiping out bits of information) and not to the processing of bits. Landauer showed that for every bit of information that is erased during an irreversible logic computation KTln2 joules of heat energy is generated, where K is the Boltzmann constant and T is the temperature in Kelvin at which the system is operating. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components. In 1965, according to 'Moore's law', stated by Gordon Moore, Intel Co-founder, the performance of integrated circuits improve at an exponential rate with the performance per unit cost increasing by a factor of 2 every 18 months.

This resulted in shrinking the dimensions on integrated structures to make it possible to operate at higher speed for the same power per unit area [1]. One should not forget that there is a minimum of quantum energy associated with elementary events which puts a fundamental limit on the miniaturization. So the question is, will Moore's law going to end? Using current technology more and more components are getting packed onto the chip and at the same time the power dissipation in the present day computer is very high. So, one of the major current research trends is towards saving of the power. Later C. H. Bennett, in 1973, showed that in order to avoid KTln2 joules of energy dissipation in a circuit it must be built from reversible circuits [3]. Reversible logic ensures zero information loss and low power dissipation. Groups like the Semiconductor Industries Association (SIA) [4], in their annual study report called the International Technology Roadmap for Semiconductors (ITRS) predict that many areas where technological breakthroughs will be needed to ensure continued progress in the field computation.

Reversible logic is one such breakthrough to carry the Moore's law into the future computing. This has motivated many research scholars and scientists to explore the area of reversible logic from various perspectives. This resulted in shrinking the dimensions on integrated structures to make it possible to operate at higher speed for the same power per unit area [1]. One should not forget that there is a minimum of

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Groups like the Semiconductor Industries Association (SIA) [4], in their annual study report called the Interna-tional Technology Roadmap for Semiconductors (ITRS) predict that many areas where technological break-throughs will be needed to ensure continued progress in the field computation. Reversible logic is one such breakthrough to carry the Moore's law into the future computing.This has motivated many research scholars and scientists to explore the area of reversible logic from various perspectives.

In the present work 4-bit multiplier circuit is construct-ed using the multi-control input Toffoli synthesis. Tof-foli gate is an universal reversible gate and it is used very frequently for the synthesis of a reversible circuit compared to the other gates like Fredkin gate. Toffoli gate synthesis is known to result in a minimum cost circuit, a primary goal of optimization. The reversible logic circuit synthesised usually results in a circuit with higher cost. The reversible logic gates used for the con-struction of a circuit needs to be implemented using universal gates.

This design is presented in this paper which is organized as follows: In Section 2 basic reversible logic gates are discussed. In section 3, the new reversible logic gate,

BVPPG gate which is implemented using Toffoli gates is discussed. In Section 4, the design 4-bit multiplier using optimized reversible logic gates and its Toffoli synthe-sis is presented. In section 5 comparison of the design with the other existing designs is presented. Section 6 presents conclusions with scope for further research.

## 2. REVERSIBLE LOGIC GATES:

A reversible logic gate is an n-input, n-output logic de-vice with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits, direct fan-out is not al-lowed as one–to-many concept is not reversible. How-ever fan-out in reversible circuits is achieved using ad-ditional gates. A reversible circuit should be designed using minimum number of reversible logic gates. So an optimized design of a reversible logic circuit is very im-portant to have the best cost metrics. The important cost metrics [5] which are used to measure the perfor-mance of a reversible logic circuit are,

- Gate count-GC- The number of reversible gates used in circuit.
- Line count-LC- Number of circuit lines
- Quantum cost- QC - Cost of the circuit in terms of the cost of a primitive gate.
- Garbage outputs- GO - Number of unused outputs present in a reversible logic circuit

### 2.1. Basic Reversible logic gates

#### 2.1.1 Feynman Gate

Figure 1 shows a 2*2 Feynman gate [6]. Quantum cost of a Feynman gate is 1.Feynman gate is called as Con-trolled NOT gate or CNOT gate. It is equivalent to single control input Toffoli gate.

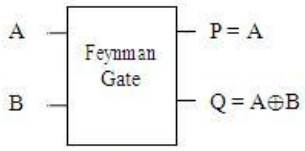


Figure 1: Feynman gate and its symbolic representation

#### 2.1.2. Toffoli Gate:

Figure 2 shows a 3*3 Toffoli gate [7] The input vector is I(A, B, C) and the output vector is O(P,Q,R). The out-puts are defined by P=A, Q=B, R=ABC. Quantum cost of a Toffoli gate is 5. It has two control inputs.

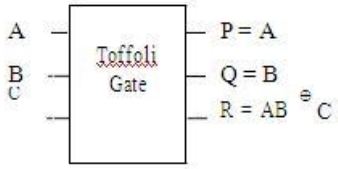


Figure 2: Toffoli gate and its symbolic representation

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### 2.1.3. Peres Gate:

Figure 3 shows a 3*3 Peres gate [8]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = AB and R=ABC. Quantum cost of a Peres gate is 4. It is needs two Toffoli gates for its construction.

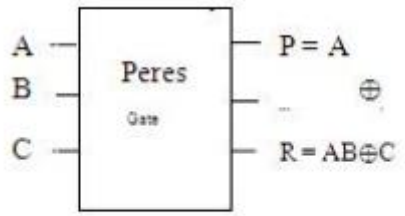



Figure 3. Peres gate and its Toffoli gate representation

## 3. NEW REVERSIBLE LOGIC GATE

### 3.1 BVPPG gate

BVPPG gate is a 5 * 5 reversible gate and its logic di-agram is as shown in figure 6. Its quantum cost is 10.

Ffoli representation of the BVPPG gate is a shown in the figure 7. The truth table of BVPPG is as shown in the Table -1.

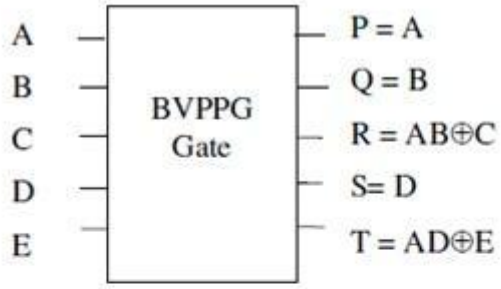
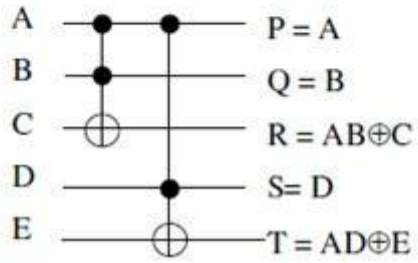


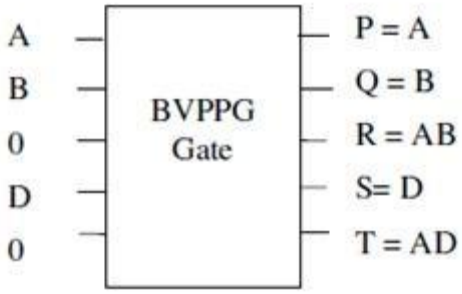

Figure 6. BVPPG gate




The BVPPG gate is used to construct the partial product generator which has resulted in least number of gates, least quantum cost and least number of garbage out-puts. The two product terms are available at the out-puts R and T of the BVPPG gate with C and E inputs maintained constant at 0.

The other outputs namely P, Q and S are used for fan-out of the multiplier operands as shown in figure 8..

This reduces the number of external fan-out gates to zero in our design which is main design feature. The proposed design is compared with the existing designs [11-22].



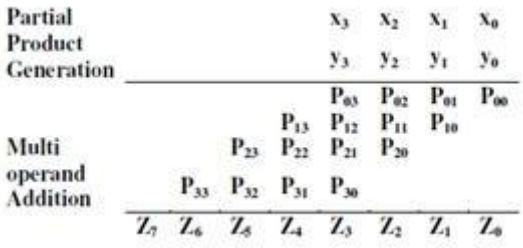

## 4. DESIGN OF 4-BIT MULTIPLIER:

Multipliers are very important in various processing steps of a computational operation. There are differ-ent approaches of a multiplier design using reversible logic gates [11-22]. The proposed multiplier uses paral-lel multiplier consists of two steps.

- Part I: Partial Product Generation (PPG)
- Part II: Multi-Operand Addition (MOA)

The operation of a 4*4 reversible multiplier is shown in figure 9. It consists of 16 Partial product bits of the

X and Y inputs to perform 4 * 4 multiplications. How-ever, it can extended to any other n * n reversible multiplier.



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### 4.1 Partial Product Generator (PPG):

The proposed design of a 4 x 4 multiplier circuit in re-versible logic requires 4 copies of each operand bit. In the existing literature on multiplier [13-16] operand bits are copied using 24 Feynman gates and in [14] the fan-out of input operands is achieved using 12 BVF gates. In [11] built-in fan-out using Toffoli gates and Peres gates is used .But in the proposed multiplier design duplica-tion of the operands is achieved without using external fan-out gates. BVPPG gates are used instead of Peres gates [12] for the construction of partial product gen-erator. The BVPPG gate is a 5 x 5 reversible logic gate and has a quantum cost of 10. It has a unique feature that it can pass through three inputs. Also it can pro-duce two product terms simultaneously with two con-stant inputs.

This feature of BVPPG gate reduces the number of re-versible gates of the circuit compared to the designs of [12-22]. The figure 10 shows the partial product gen-erator using new BVPPG gates. The new BVPPG gate is similar to a double Toffoli gate or it is equal to a Toffoli gate with 4 control inputsThe input operands x3, x2, x1, x0 and y3, y2, y1, y0 are used directly and only once.

The BVPPG gate outputs the operands along with the product terms which are used as inputs to the next BVPPG gate to generate other product terms. To the best of our knowledge ours is the first design to get partial products without using fan-out gates with only 8 reversible gates and also to construct the Toffoli gate structure of the multiplier. In paper [12], 7 Peres gates and 9 Toffoli gates are used to generate the product terms without fan-out gates but number of gates is more than that used in our design.

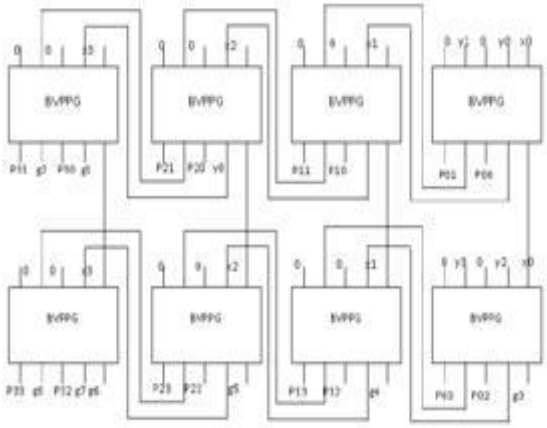

Fig: Partial product generator using BVPPG gates

The Toffoli gate implementation of the partial product generator obtained using RevKit-tool [9, 10, 23] is as shown in the

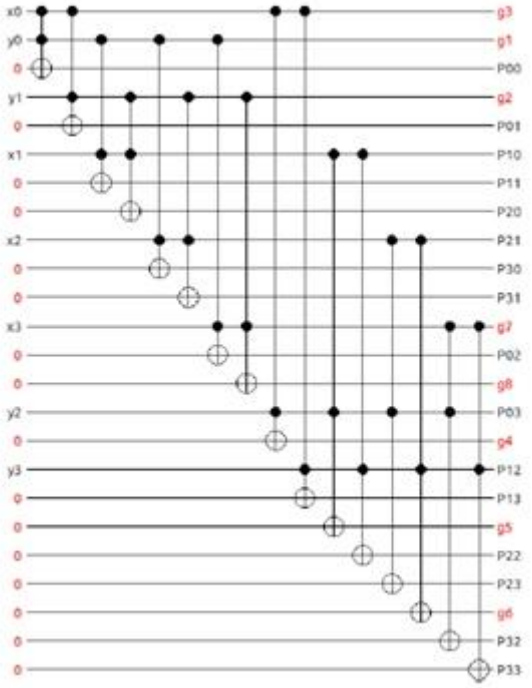

Fig: . Four operand addition circuit-MOA

### 4.2. Multi-Operand Addition (MOA):

As proposed in [8], to implement an n operand addition circuit part a carry save adder (CSA) is used. The CSA tree reduces the four operands to two. Thereaf-ter, a Carry Propagating Adder (CPA) adds these two operands and produces the final 8-bit product. The proposed four operand adder shown in the figure 13 uses DPG gate as a reversible full adder and Peres gate as half adder.

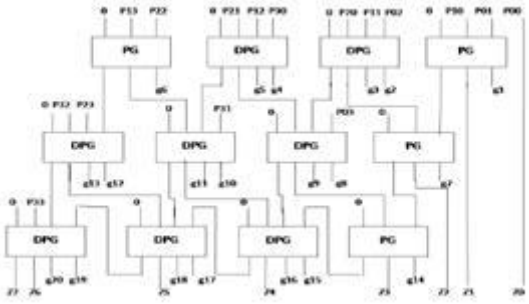

Fig: . Toffoli cascade of multi-operand adder(MOA) block.

The existing 4*4 gates namely DPG [12], HNG [13], PFAG [14], MKG [15] and TSG [16], and can be

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individu-ally used as an adder. It is shown that use of DPG gate [12] reduces the quantum cost of the multiplier to a minimum value.

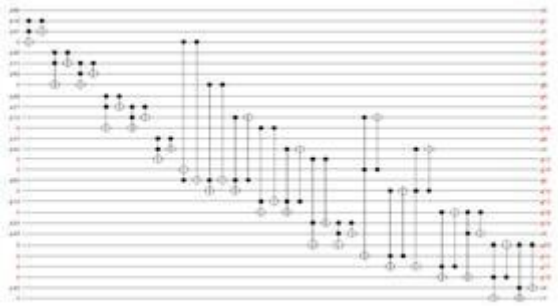

Fig: Toffoli cascade of Partial product generator using BVPPG gates

## 5. PROPOSED SYSTEM: COMPLUX MULTIPLIER DESIGNS:

In this paper complex Multiplier design is done using compressors and. Multiplication Algorithm The Complex multiplier design and its functionality were discussed in the previous chapters. Now this chapter deals with the simulation and synthesis results of the Complex multiplier. Here Modelsim tool is used in order to simulate the design and checks the functionality of the design.

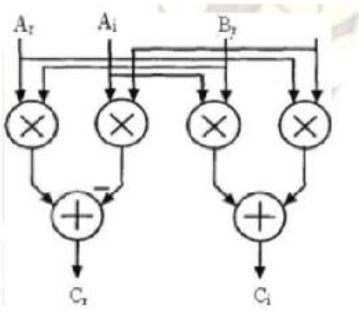


Fig: implementation of complex multiplier

## 6. RESULTS AND DISCUSSION:

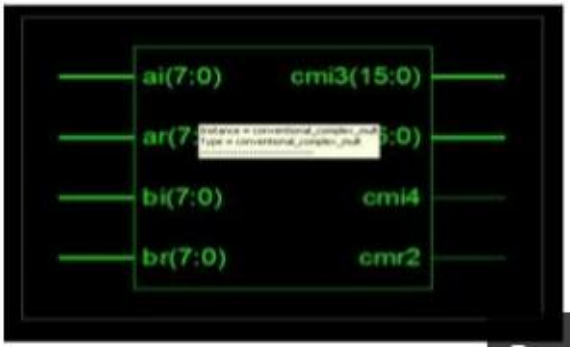


Fig: RTL Diagram of conventional complex multiplier

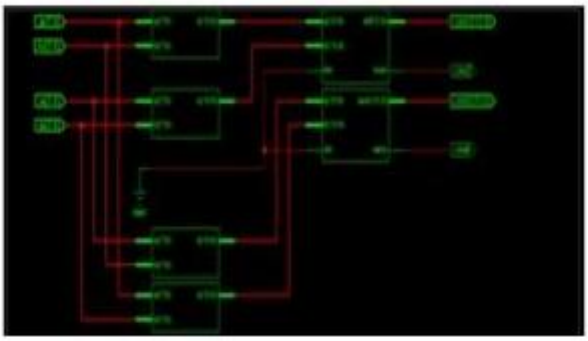

Fig: Internal Diagram of conventional complex multiplier:

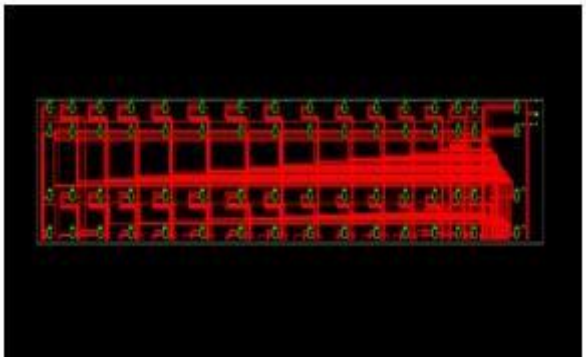

Fig: Technology diagram

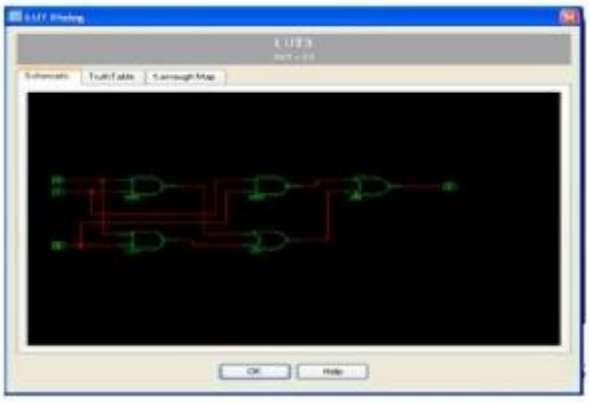

Fig: LUT diagram

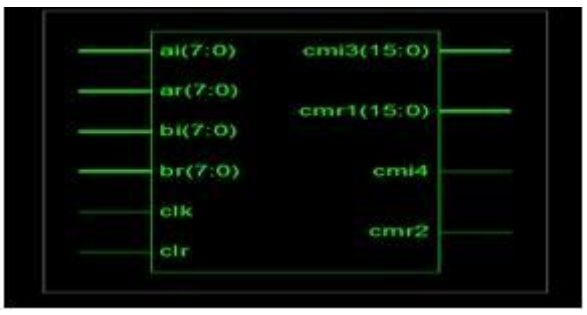


Fig:Proposed system

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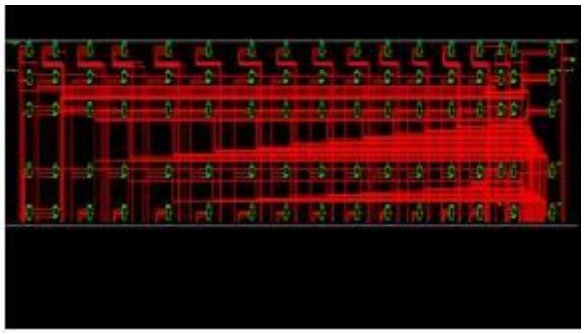

Fig:Technology diagram

## 7. CONCLUSIONS:

The focus of this paper is the application of a reversible logic gate to realize a 4-bit multiplier using a new reversible logic gate which is designed keeping in view the optimization factors of the reversible circuits and is synthesized using Xilinx synthesis using Complex Mul-tipliers.

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