ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Reliable Low Power Multiplier Design Using Fixed Width Reduced Precision Replica Block

Kadiri Mrunalini
M.Tech Student
Stanley Stephen college of Engineering & Technology, Panchalingala, Kurnool – 518004. A.P.

N.Praveen Kumar, M.Tech, (Ph.D),
Associate Professor
Stanley Stephen college of Engineering & Technology, Panchalingala, Kurnool – 518004. A.P.

Abstract

In this paper, we propose a reliable low-power multiplier design by adopting algorithmic noise tolerant (ANT) architecture with the fixed-width multiplier to build the reduced precision replica redundancy block (RPR). The proposed ANT architecture can meet the demand of high precision, low power consumption, and area efficiency. We design the fixed-width RPR with error compensation circuit via analyzing of probability and statistics. Using the partial product terms of input correction vector and minor input correction vector to lower the truncation errors, the hardware complexity of error compensation circuit can be simplified. In a 12 × 12 bit ANT multiplier, circuit area in our fixed-width RPR can be lowered by 44.55% and power consumption in our ANT design can be saved by 23% as compared with the state-of-art ANT design.

Index Terms— Algorithmic noise tolerant (ANT), fixed-width multiplier, reduced-precision replica (RPR), voltage overscaling (VOS).

I. INTRODUCTION

The rapid growth of portable and wireless computing systems in recent years drives the need for ultralow power systems. To lower the power dissipation, supply voltage scaling is widely used as an effective low-power technique since the power consumption in CMOS circuits is proportional to the square of supply voltage. However, in deep-sub micrometer process technologies, noise interference problems have raised difficulty to design the reliable and efficient microelectronics systems; hence, the design techniques to enhance noise tolerance have been widely developed.

An aggressive low-power technique, referred to as voltage overscaling (VOS), was proposed to lower supply voltage beyond critical supply voltage without sacrificing the throughput. However, VOS leads to severe degradation in signal-to-noise ratio (SNR). A novel algorithmic noise tolerant (ANT) technique combined VOS main block with reduced-precision replica (RPR),which combats soft errors effectively while achieving significant energy saving. However, the RPR designs in the ANT designs are designed in a customized manner, which are not easily adopted and repeated. The RPR designs in the ANT designs can operate in a very fast manner, but their hardware complexity is too complex.

As a result, the RPR design in the ANT design is still the most popular design because of its simplicity. However, adopting with RPR should still pay extra area overhead and power consumption.

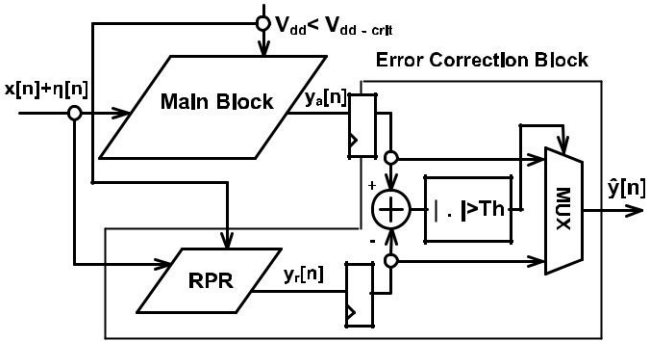

Fig. 1.ANT architecture.

In this paper, we further proposed an easy way using the fixed-width RPR to replace the full-width RPR block . Using the fixed-width RPR, the computation error can be corrected with lower power consumption and lower area overhead. We take use of probability, statistics, and partial product weight analysis to find

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

the approximate compensation vector for a more precise RPR design. In order not to increase the critical path delay, we restrict the compensation circuit in RPR must not be located in the critical path. As a result, we can realize the ANT design with smaller circuit area, lower power consumption, and lower critical supply voltage.

II. ANT ARCHITECTURE DESIGNS

The ANT technique includes both main digital signal processor (MDSP) and error correction (EC) block, as shown in Fig. 1. To meet ultralow power demand, VOS is used in MDSP. However, under the VOS, once the critical path delay T_{cp} of the system becomes greater than the sampling period T_{samp}, the soft errors will occur. It leads to severe degradation in signal precision. In the ANT technique, a replica of the MDSP but with reduced precission operands and shorter computation delay is used as EC block. Under VOS, there are a number of input-dependent soft errors in its output $y_a[n]$; however, RPR output y_r $[n]$is still correct since the critical path delay of the replica is smaller than $T_{samp.}$ Therefore $y_r[n]$ is applied to detect errors in the MDSP output $y_a[n]$.

Error detection is accomplished by comparing the difference $| y_a[n] - y_r [n] |$ against a threshold *Th*. Once the difference between $y_a[n]$ and y_r $[n]$ is larger than *Th*, the output $\hat{y}[n]$ is y_r $[n]$ instead of $y_a[n]$. As a result, $\hat{y}[n]$ can be expressed as

$$\hat{y}[n] = \begin{cases} y_a\ [n]\ ,\text{if}\ |\ y_a\ [n] - y_r\ [n]\ |\ \leq\ Th \\ y_r\ [n]\ ,\text{if}\ |\ y_a\ [n] - y_r\ [n]\ |\ >\ Th. \end{cases} \quad (1)$$

Th is determined by

$$Th = \max_{\forall input} |\ yo\ [n]\ -\ yr[n]\ | \quad (2)$$

Where $y_o[n]$ is error free output signal. In this way, the power consumption can be greatly lowered while the SNR can still be maintained without severe degradation.

III. PROPOSED ANT MULTIPLIER DESIGN USING FIXED-WIDTH RPR

In this paper, we further proposed the fixed-width RPR to replace the full-width RPR block in the ANT design, as shown in Fig. 2, which can not only provide higher computation precision, lower power consumption, and lower area overhead in RPR, but also perform with higher SNR, more area efficient, lower operating supply voltage, and lower power consumption in realizing the ANT architecture. We demonstrate our fixed-width RPR-based ANT design in an ANT multiplier.

The fixed-width designs are usually applied in DSP applications to avoid infinite growth of bit width. Cutting off *n*-bit least significant bit (LSB) output is a popular solution to construct a fixed-width DSP with *n*-bit input and *n*-bit output. The hardware complexity and power consumption of a fixed-width DSP is usually about half of the full-length one. However, truncation of LSB part results in rounding error, which needs to be compensated precisely. Many literatures have been presented to reduce the truncation error with constant correction value or with variable correction value. The circuit complexity to compensate with constant corrected value can be simpler than that of variable correction value; however, the variable correction approaches are usually more precise.

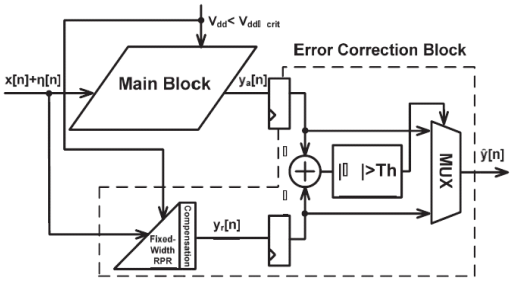

Fig. 2. Proposed ANT architecture with fixed- width RPR.

Compensation method is to compensate the truncation error between the full-length multiplier and the fixed-width multiplier. However, in the fixed-width RPR of an ANT multiplier, the compensation error we need to correct is the overall truncation error of MDSP block.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Our compensation method is to compensate the truncation error between the full-length MDSP multiplier and the fixed-width RPR multiplier. In nowadays, there are many fixed-width multiplier designs applied to the full-width multipliers. However, there is still no fixed-width RPR design applied to the ANT multiplier designs.

To achieve more precise error compensation, we compensate the truncation error with variable correction value. We construct the error compensation circuit mainly using the partial product terms with the largest weight in the least significant segment. The error compensation algorithm makes use of probability, statistics, and linear regression analysis to find the approximate compensation value. To save hardware complexity, the compensation vector in the partial product terms with the largest weight in the least significant segment is directly inject into the fixed-width RPR, which does not need extra compensation logic gates . To further lower the compensation error, we also consider the impact of truncated products with the second most significant bits on the error compensation. We propose an error compensation circuit using a simple minor input correction vector to compensation the error remained. In order not to increase the critical path delay, we locate the compensation circuit in the noncritical path of the fixed-width RPR. As compared with the full-width RPR design, the proposed fixed-width RPR multiplier not only performs with higher SNR but also with lower circuitry area and lower power consumption.

A. Proposed Precise Error Compensation Vector for Fixed-Width RPR Design

In the ANT design, the function of RPR is to correct the errors occurring in the output of MDSP and maintain the SNR of whole system while lowering supply voltage. In the case of using fixed-width RPR to realize ANT architecture, we not only lower circuit area and power consumption, but also accelerate the computation speed as compared with the conventional full-length RPR. However, we need to compensate huge truncation error due to cutting off many hardware elements in the LSB part of MDSP. In the MDSP of *n*-bit ANT Baugh–Wooley array multiplier, its two unsigned *n*-bit inputs of *X* and *Y* can be expressed as

$$X = \sum_{i=0}^{n-1} x_i \ 2^i, Y = \sum_{j=0}^{n-1} y_j \ 2^j \qquad (3)$$

The multiplication result *P* is the summation of partial products of $x_i y_j$, which is expressed as

$$P = \sum_{k=0}^{2n-1} p_k \ 2^k = \sum_{j=0}^{n-1} \sum_{i=0}^{n-1} x_i \ y_j \ 2^{i+j} \qquad (4)$$

The (*n*/2)-bit unsigned full-width Baugh–Wooley partial product array can be divided into four subsets, which are most significant part (MSP), input correction vector [ICV(*β*)], minor ICV [MICV(*α*)], and LSP, as shown in Fig. 3. In the fixed-width RPR, only MSP part is kept and the other parts are removed.

Therefore, the other three parts of ICV(*β*), MICV(*α*), and LSP are called as truncated part. The truncated ICV(*β*) and MICV(*α*) are the most important parts because of their highest weighting. Therefore, they can be applied to construct the truncation error compensation algorithm.

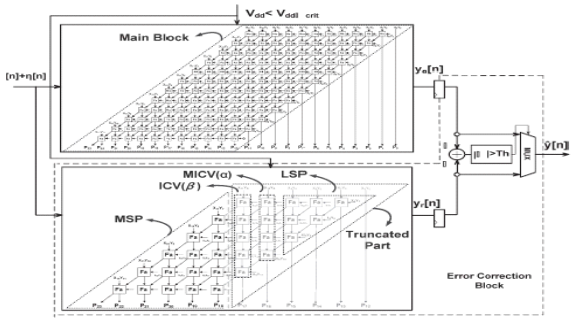

Fig. 12 × 12 bit ANT multiplier is implemented with the six-bit fixed-width replica redundancy block.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

To evaluate the accuracy of a fixed-width RPR, we can exploit the difference between the (*n*/2)-bit fixed-width RPR output and the 2*n*-bit full-length MDSP output, which is expressed as

$$\varepsilon = P - P_t \qquad (5)$$

where P is the output of the complete multiplier in MDSP and P_t is the output of the fixed-width multiplier in RPR. P_t can be expressed as

$$\begin{aligned} P_t &= \sum_{j=\frac{n}{2}+1}^{n-1} y_j 2^j \sum_{j=\frac{3n}{2}-j}^{n-1} x_i 2^i \\ &+ f\left(x_{n-1}\, y_{\frac{n}{2}}, x_{n-2}\, y_{\frac{n}{2}+1}, x_{n-3}\, y_{\frac{n}{2}+2}, \ldots, x_{\frac{n}{2}}\, y_{\frac{n}{2}+2}\right) \\ &+ f\left(x_{n-2}\, y_{\frac{n}{2}}, x_{n-3}\, y_{\frac{n}{2}+1}, x_{n-4}\, y_{\frac{n}{2}+2}, \ldots, x_{\frac{n}{2}}\, y_{\frac{n}{2}-2}\right) \\ &= \sum_{j=\frac{n}{2}+1}^{n-1} y_j 2^j \sum_{j=\frac{3n}{2}-j}^{n-1} x_i 2^i + f(ICV) + f(MICV) \\ &= \sum_{j=\frac{n}{2}+1}^{n-1} y_j 2^j \sum_{j=\frac{3n}{2}-j}^{n-1} x_i 2^i + f(EC) \qquad (6) \end{aligned}$$

where f (EC) is the error compensation function, f(ICV) is the error compensation function contributed by the input correction vector ICV(β), and f (MICV) is the error compensation function contributed by minor input correction vector MICV(α).

The source of errors generated in the fixed-width RPR is dominated by the bit products of ICV since they have the largest weight. It is reported that a low-cost EC circuit can be designed easily if a simple relationship between f (EC) and β is found.

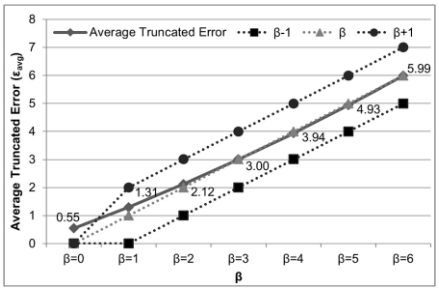

Fig. 4. Statistical curves of average truncation error in the LSP block and the curves of compensation function with β− 1, β, and β + 1 in the 12-bit fixed-width RPR-based ANT multiplier

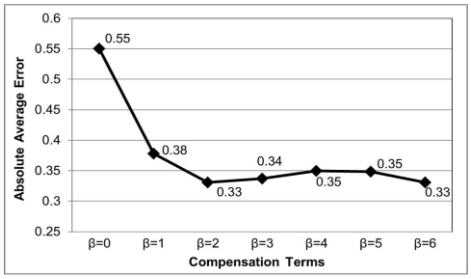

Fig. 5. Analysis of absolute average compensation error under various β values in the 12-bit fixed-width RPR-based ANT based ANT multiplier.

It is noted that β is the summation of all partial products of ICV. By statistically analyzing the truncated difference between MDSP and fixed-width RPR with uniform input distribution, we can find the relationship between f (EC) and β. As shown in Fig. 4, the statistical results show that the average truncation error in the fixed-width RPR multiplier is approximately distributed between β and β +1. More precisely, as β = 0, the average truncation error is close to β + 1. As β> 0, the average truncation error is very close to . If we can select β as the compensation vector, the compensation vector can directly inject into the fixed-width RPR as compensation, which does not need extra compensation logic gates.

We go further to analyze the compensation precision by selecting β as the compensation vector. We can find that the absolute average error in β = 0 is much larger than that in other β cases, as shown in Fig. 5. Moreover, the absolute average error in β = 0 is larger than $0.5^* 2^{(3n/2)}$, while the absolute average error in other β situations is smaller than $0.5^* 2^{(3n/2)}$. Therefore, we can apply multiple input error compensation vectors to further enhance the error compensation precision. For the β > 0 case, we can still select β as the compensation vector. For the β = 0 case, we select β+1 combining with MICV as the compensation vector.

Before directly injecting the compensation vector β into the fixed-width RPR, we go further to double check the weight for the partial product terms in ICV with the same partial product summation value β but

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

with different locations. As shown in Table I, the average error value for each ICV vector with the same partial product term summation value is Relation between the partial product term's location in icv and the statistical compensation error e_{avg}

TABLE I

Relation between the partial product term's location in icv and the statistical compensation error e_{avg}

Row	ICV	E_{avg}	F(ICV)
1	(1,0,0,0,0,0)	1.328	1
2	(0,1,0,0,0,0)	1.303	1
3	(0,0,1,0,0,0)	1.293	1
4	(0,0,0,1,0,0)	1.293	1
5	(0,0,0,0,1,0)	1.303	1
6	(0,0,0,0,0,1)	1.328	1

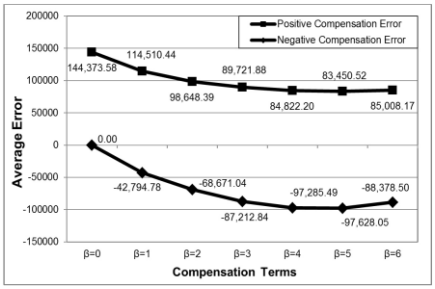

Fig. 6. Analysis of average positive and negative compensation error under various β values in the 12-bit fixed-width RPR-based ANT multiplier

Nearly the same even their partial product term's location is different. That is to say that no matter ICV = (1,0,0,0,0,0), ICV = (0,1,0,0,0,0), ICV = *(*0, 0, 1, 0, 0, 0*)*, ICV = *(*0, 0, 0, 1, 0, 0*)*, ICV = *(*0, 0, 0, 0, 1, 0*)*, or ICV = *(*0, 0, 0, 0, 0, 1*)*, their weight in each partial product term for truncation error compensation is nearly the same. Therefore, we apply the same weight of unity to each input correction vector element. This conclusion is beneficial for us to inject the compensation vector β into the fixed-width RPR directly. In this way, no extra compensation logic gates are needed for this part compensation and only wire connections are needed.

For the $\beta = 0$ case, we go further to analyze the error profile in the ICV and MICV. In ICV, we can find that all the truncation errors are positive when $\beta = 0$, as shown in Fig. 6.

It implies us that if we adopt the multiple compensation vectors for the average compensation error terms are larger than $0.5^* 2^{(3n/2)}$, we can lower the compensation error effectively and no additional compensation error will be generated. The multiple compensation vectors are constructed by ICV(β) combined with MICV(α). The weight of MICV(α) is only half of ICV(β). The summation of all partial products of MICV(α), which is denoted as β_l , have four possible values of 0, 1, 2, and 3 as $n = 12$ and $\beta = 0$.

In Fig. 7, the statistical results show that the average truncation error contributed by the MICV in the case of $\beta = 0$ is approximately proportional to α. Moreover, the absolute average truncation error in the situation of $\alpha = 0$ is smaller than $0.5^* 2^{(3n/2)}$, while the absolute average truncation error in the situation of $\beta_l > 0$ is larger than $0.5^* 2^{(3n/2)}$. For the case of the absolute average truncation error is smaller than $0.5^* 2^{(3n/2)}$, $\beta_l = 0$, selecting β as the compensation vector is suitable.

$$f(\mathrm{ICV}) = \begin{cases} 0, & \text{if } \beta_1 = 0 \\ \beta, & \text{if } \beta_1 = 1, \text{ or } \beta_1 = 2 \ \& \ (\text{up-MICV} \neq 0 \ \& \ \text{down-MICV} \neq 0) \\ \beta\text{-}1, & \text{if } \beta_1 = 2 \ \& \ (\text{up-MICV} \neq 0 \text{ or down-MICV} = 0), \beta_1 = 3, \\ & \quad \text{or } \beta_1 = 4 \ \& \ (\text{up-MICV} \neq 0 \ \& \ \text{down-MICV} \neq 0) \\ \beta\text{-}2, & \text{if } \beta_1 = 4 \ \& \ (\text{up-MICV} = 0 \text{ or down-MICV} = 0) \end{cases} \quad (7)$$

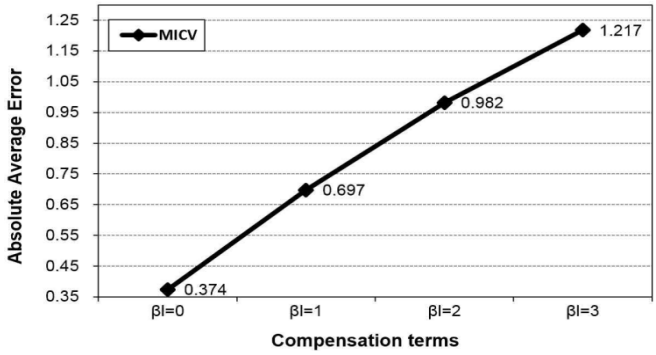

Fig. 7. Analysis of absolute average compensation error under various βl values while β = 0 in the 12-bit fixed-width RPR-based ANT multiplier

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

However, for the case of the absolute average truncation error is larger than $0.5^* 2^{(3n/2)}$, selecting β as the compensation vector is not suitable since insufficient error compensation will occur. Therefore, we adopt ICV together with MICV to amend this insufficient error compensation case when $\beta = 0$ and $\beta_l > 0$ as well. If $\beta = 0$ is contributed by $\beta_l > 0$, we will inject one more carry-in compensated vector in the weight of $2^{(3n/2)}$. In this way, we can remove the cases of $|\varepsilon| > 0.5^* 2^{(3n/2)}$ effectively.

Finally, the proposed error compensation algorithm is expressed as equ (7).

As shown in Fig. 8, we can demonstrate that the compensation error is effectively lowered by adopting ICV together with MICV while comparing with the case of fixed-width RPR only applying the compensation vector of β and with the case of full-width RPR.

B. Proposed Precise Error compensation Vector for Fixed-width RPR Design

To realize the fixed-width RPR, we construct one directly injecting ICV (β) to basically meet the statistic distribution and one minor compensation vector MICV(α) to amend the insufficient error compensation cases. The compensation vector ICV(β) is realized by directly injecting the partial terms of $^X n{-}1^Y n/2$, $^X n{-}2^Y(n/2){+}1$, $^X n{-}3^Y(n/2){+}2$, . . . , $^X (n/2){+}2^Y n{-}2$.

These directly injecting compensation terms are labeled as $C_1, C_2, C_3, \ldots, C_{(n/2)-1}$ in Fig. 9. The other compensation vector used to mend the insuf One input of OR gate is injected by $X_{(n/2)}Y_{n-1}$, which is designed to realize the function of compensation vector β . The other input is conditional controlled by the judgment formula used to judge whether $\beta = 0$ and $\beta_l = 0$ as well. As shown in Fig. 8, the term Cm1 is used to judge whether $\beta = 0$ or not. The judgment function is realized by one NOR gate, while its inputs are $^X n{-}1^Y n/2$, $^X n{-}2^Y(n/2){+}1$, $^X n{-}3^Y(n/2){+}2$, . . . , $^X (n/2){+}2^Y n{-}2$. The term C_{m2} is used to judge whether $\beta_l = 0$. The judgment function is realized by one OR gate, while its inputs are $^X n{-}2^Y n/2$, $^X n{-}3^Y(n/2){+}1$, $^X n{-}4^Y(n/2){+}2$, . . . , $^X (n/2){+}1^Y n{-}2$. If both of these two judgments are true, a compensation term C_m is generated via a two-input AND gate. Then, C_m is injected together with $X_{(n/2)}Y_{n-1}$ into a two-input OR gate to correct the insufficient error compensation.

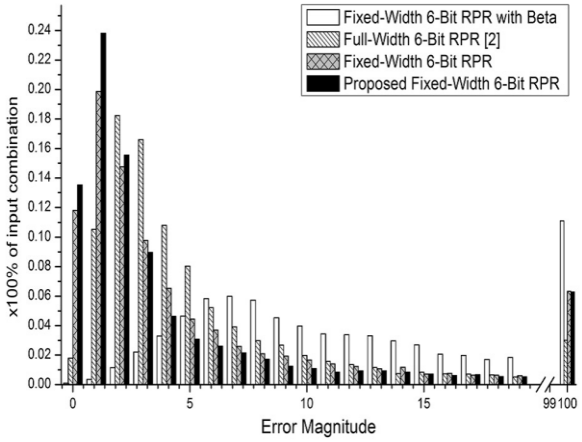

Fig. 8. Comparison of absolute error between the proposed design, the fixedwidth RPR with compensation vectorβ only, and the full-width RPR in the 12-bit fixed-width RPR-based ANT multiplier.

Moreover, the carry-in signal $C_{(n/2)}$ is injected in the bottom of error compensation vector, which is the farthest location away from the critical path.

Therefore, not only the error compensation precision in the fixed-width RPR can be enhanced, the computation delay will also not be postponed. Since the critical supply voltage is dominated by the critical delay time of the RPR circuit, preserving the critical path of RPR not be postponed is very important. Finally, the proposed high-precision fixed-width RPR multiplier circuit is shown in Fig. 9.

In our presented fixed-width RPR design, the adder cells can be saved by half as compared with the conventional full-width RPR. Moreover, the proposed high-precision fixed-width RPR design can even provide higher precision as compared with the full-width RPR design.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

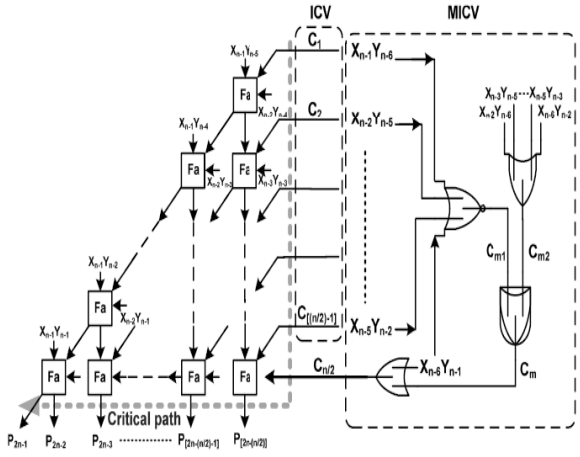

Fig 9. Proposed high-accuracy fixed-width RPR multiplier with compensation constructed by the multiple truncation EC vectors combined ICV together.

IV. SIMULATION RESULT

In simulation results we compare device utilization (area efficiency**)** and delay for both array multiplier and booth multiplier, using Xilinx ISE and Model Sim softwares.

LOGIC DIAGRAMS:

16-bit Array Multiplier:

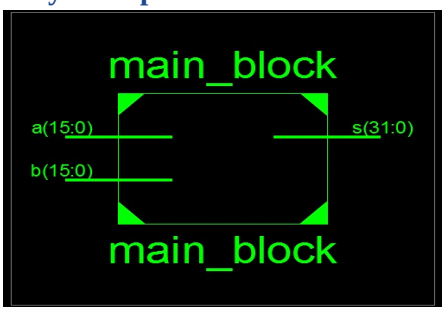

Fig10. Logic Diagram of 16-Bit Array Multiplier

16-bit Booth Multiplier:

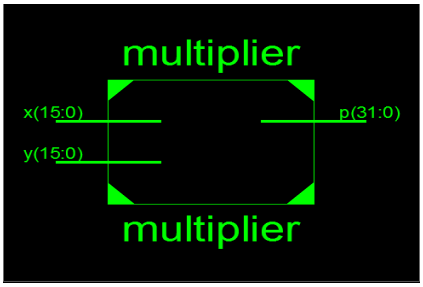

Fig11. Logic Diagram of 16-Bit Booth Multiplier

RPR Block:

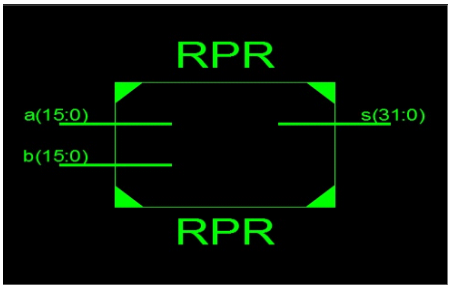

Fig13 Logic Diagram of Fixed Width RPR Block

RTL Schematics:

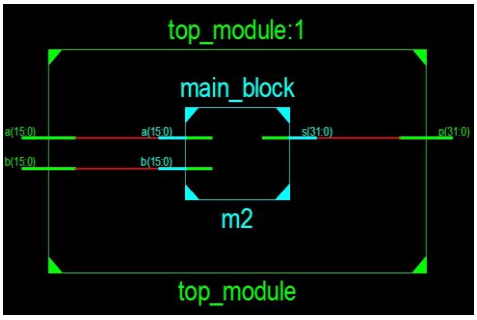

Fig13 RTL Schematic of 16-Bit Array Multiplier

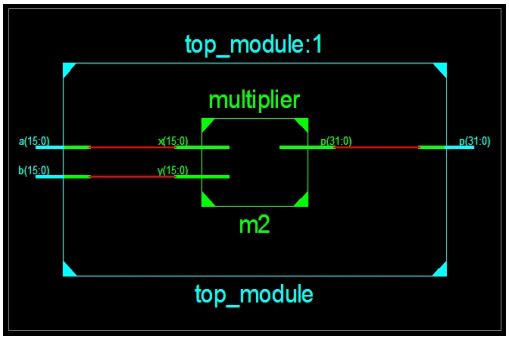

Fig.14 RTL Schematic of 16-Bit Booth Multiplier

Device utilization summary fo16-bit multiplies:

DEVICE UTILIZATION SUMMARY(ESTIMATED VALUES)			
Logic utilization	**Used**	**Available**	**Utilization**
Number of slices	379	4656	8%
Number of 4inputs LUTs	667	9312	7%
Number of bonded IOBs	64	232	27%

Table: Device Utilization of 16-Bit Array Multiplier

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

DEVICE UTILIZATION SUMMARY(ESTIMATED VALUES)			
Logic utilization	**Used**	**Available**	**Utilization**
Number of slices	289	4656	8%
Number of 4inputs LUTs	533	9312	7%
Number of bonded IOBs	64	232	27%

Table: Device Utilization of 16-Bit Booth Multiplier

Simulation report:

Delay Analysis

The synthesis of the above mentioned multipliers is done in Xilinx tool ISE 13.2. The delay parameters are being compared between RPR unit using different multipliers and then tabulated.

Typeof multiplier	Delay without RPR in ns	Total delay with RPR in ns
array multiplier	63.394	63.655
booth multiplier	36.318	36.618

Table: Comparison of 16-bit multipliers in terms of delay

RPR unit with	NO.of slices	NO. of 4 input lut's
Array multiplier	379	667
Booth multiplier	289	533

Table: Device utilization summary for RPR unit using 16-bit multipliers

Simulation results:

Simulation result for 16-bit Array Multiplier with RPR unit.

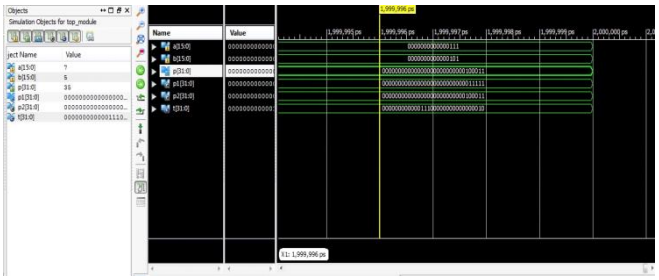

Fig.15 Simulated wave forms for 16-bit Array Multiplier design with RPR

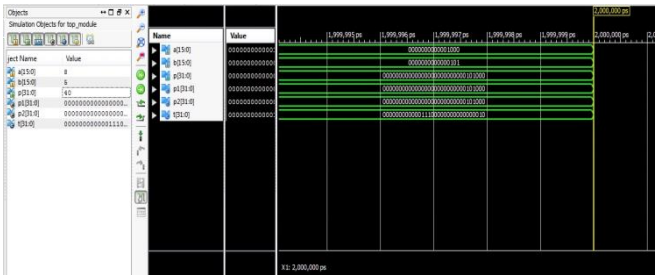

Fig 16 Simulated wave forms for 16-bit Booth Multiplier design with RPR

V. CONCLUSION

A low error and area-efficient fixed width RPR based ANT multiplier design is implemented. Noise sources such as cosmic rays and alpha particles can impact the error control blocks as well. We have proposed novel algorithmic noise tolerant technique referred to as reduced precision redundancy (RPR) to combat errors in hardware. ANT is an elegant technique to increase SNR. While using 16-bit Array multiplier with RPR unit, the delay is 63.655ns and number of slice is 379. However, the 16- bit Booth multiplier with RPR unit gives delay of 36.618ns and reduced number of slices (i.e 289). Hence, Booth multiplier with RPR unit reduces delay to half and number of slices is also reduced as compared to Array multiplier.

REFERENCES

[1] B. Shim, S. Sridhara, and N. R. Shanbhag, "Reliable low-power digital signal processing via reduced precision redundancy," IEEE Trans.Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 5, pp. 497–510,May 2004.

[2] B. Shim and N. R. Shanbhag, "Energy-efficient soft-error tolerant digital signal processing," IEEE Trans. Very Large Scale Integr. (VLSI) Syst.vol. 14, no. 4, pp. 336–348, Apr. 2006.

[3] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, "Low-power digital signal processing using approximate adders," IEEE Trans. Comput Added Des. Integr. Circuits Syst., vol. 32, no. 1, pp. 124–137, Jan. 2013.

[4] Y. Liu, T. Zhang, and K. K. Parhi, "Computation error analysis in digital signal processing systems with overscaled supply voltage," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 18, no. 4, pp. 517–526,Apr. 2010.

[5] J. N. Chen, J. H. Hu, and S. Y. Li, "Low power digital signal processing scheme via stochastic logic protection," in Proc. IEEE Int. Symp. Circuits Syst., May 2012, pp. 3077–3080.

[6] J. N. Chen and J. H. Hu, "Energy-efficient digital signal processing via voltage-overscaling-based residue number system," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 7, pp. 1322–1332, Jul. 2013.

[7] P. N. Whatmough, S. Das, D. M. Bull, and I. Darwazeh, "Circuit-level timing error tolerance for low-power DSP filters and transforms," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 6, pp. 12–18, Feb. 2012.

[8] G. Karakonstantis, D. Mohapatra, and K. Roy, "Logic and memory design based on unequal error protection for voltage-scalable, robust and adaptive DSP systems," J. Signal Process. Syst., vol. 68, no. 3, pp. 415–431, 2012.

[9] Y. Pu, J. P. de Gyvez, H. Corporaal, and Y. Ha, "An ultra low energy/frame multi-standard JPEG co-processor in 65-nm CMOS with sub/near threshold power supply," IEEE J. Solid State Circuits, vol. 45, no. 3, pp. 668–680, Mar. 2010.

[10] H. Fuketa, K. Hirairi, T. Yasufuku, M. Takamiya, M. Nomura, H. Shinohara, et al., "12.7-times energy efficiency increase of 16-bit integer unit by power supply voltage (VDD) scaling from 1.2V to 310mV enabled by contention-less flip-flops (CLFF) and separated VDD between flip-flops and combinational logics," in Proc. ISLPED,Fukuoka, Japan, Aug. 2011, pp. 163–168.

Author Details

Kadiri Mrunalini, M.Tech, Stanley Stephen College of Engineering & Technology, Panchalingala, Kurnool – 518004. A.P.

N.Praveen Kumar, M.Tech, Ph.D, Associate Professor, Stanley Stephen College of Engineering & Technology, Panchalingala, Kurnool, AP, India.