

Hybrid Control Scheme of Phase-Shift Full-Bridge Series-Resonant Converter

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ABSTRACT

This paper exhibits a mixture sort full-connect dc/dc converter with high effectiveness. Utilizing a cross breed control plan with a basic circuit structure, the proposed dc/dc converter has a half and half operation mode. Under an ordinary info run, the proposed converter works as a stage move full-connect arrangement resounding converter that gives high effectiveness by applying delicate exchanging on all switches and rectifier diodes and lessening conduction misfortunes. At the point when the info is lower than the typical information run, the converter works as a dynamic cinch venture up converter that upgrades an operation range. Because of the half and half operation, the proposed converter works with bigger stage shift esteem than the traditional converters under the ordinary information range. Subsequently, the proposed converter is fit for being intended to give high power transformation proficiency and its operation reach is expanded. A 1kW model is actualized to affirm the hypothetical investigation and legitimacy of the proposed converter.

Index Terms— Full-bridge circuit, phase-shift control, active-clamp circuit.

I. INTRODUCTION

These days, requests on dc/dc converters with a powerful thickness, high productivity, and low electromagnetic obstruction (EMI) have been expanded in different modern fields. As the changing recurrence increments to get high power thickness, changing misfortunes identified with the turn-on and turn-off of the exchanging gadgets increment. Since

these misfortunes constrain the expansion of the exchanging recurrence, delicate exchanging procedures are key.

Among past dc/dc converters, a stage move full-connect (PSFB) converter is appealing in light of the fact that all essential switches are turned on with zero-voltage exchanging (ZVS) without extra assistant circuits [1]. Nonetheless, the PSFB converter has some difficult issues, for example, limited ZVS scope of slacking leg switches, high power misfortunes by circling current, and voltage ringing crosswise over rectifier diodes. Particularly, with a prerequisite of wide information extend, the PSFB converter is intended to work with little stage shift esteem under the typical info run; the outline of the PSFB converter protracts the freewheeling interim and causes the inordinate circling current which expands conduction misfortunes [2], [3].

As of late, the different PSFB converters utilizing helper circuits have been presented [4]-[12]. The PSFB converters develop ZVS run or diminish the flowing current by using extra uninvolved or dynamic assistant circuits. Be that as it may, the extra circuits result in convoluted circuit design, complex control methodology, and additional force misfortunes [13]. Likewise, some PSFB converters still require the additional snubber to counteract genuine voltage ringing issue crosswise over rectifier diodes. In [14], [15], the PSFB converters utilizing an arrangement thunderous converter have been presented, to be specific, the PSFB arrangement full converters; they have numerous preferences, for example, delicate exchanging systems of all essential switches and

rectifier diodes, end of flowing current, diminishment of voltage weight on rectifier diodes, and a basic circuit structure. Be that as it may, when all previously mentioned PSFB converters are required to ensure a wide operation range, regardless they work with the little stage shift esteem under the typical info range. The operation with the little stage shift esteem for the most part gives high conduction misfortunes by high pinnacle current; it brings about low influence productivity. To accomplish high effectiveness under the ordinary info range and cover the wide information run, the diverse procedures are recommended. The converters in [16], [17] change the turn proportion of the transformer by utilizing extra exchanging gadgets. Despite the fact that the methodology accomplishes high productivity and guarantees the wide information run, these strategies give circuit multifaceted nature and diminishment of the transformer use.

Dynamic cinch circuits have been generally used to assimilate surge vitality put away in spillage inductance of a transformer. Moreover, the circuits provide a soft switching technique [18], [19]. Some studies have introduced dc/dc converters combining the active-clamp circuit and voltage doubler or multiplier rectifier [20], [21]. The circuit configuration allows achieving a step-up function like a boost converter. The voltage stresses of rectifier diodes are also clamped at the output voltage and no extra snubber circuit is required.

In this paper, a novel half and half sort FB dc/dc converter with high proficiency is proposed; the converter is gotten from a mix of a PSFB arrangement thunderous converter and a dynamic cinch venture up converter with a voltage doubler circuit. Utilizing a cross breed control plan with a basic circuit structure, the proposed converter has two operation modes. Under the ordinary information go, the proposed converter works as a PSFB arrangement resounding converter. The proposed converter yields high proficiency by applying delicate exchanging strategies on all the essential switches and rectifier diodes and by lessening conduction misfortunes. At the point when

the info voltage is lower than the ordinary information go, the converter works as a dynamic cinch venture up converter. In this mode, the proposed converter gives a stage - up capacity by utilizing the dynamic cinch circuit on the essential side and the voltage doubler rectifier on the optional side. Because of the cross breed operation, the proposed converter works with bigger stage shift esteem than the routine PSFB converters under the ordinary info range. In this way, the proposed converter has the accompanying points of interest:

- 1) Under the normal input range, the proposed converter can be designed to optimize power conversion efficiency.
- 2) When the input is lower than the normal input range, the proposed converter performs a step-up function, which enhances the operation range.
- 3) Without complex circuit structures, the converter have high efficiency under the normal input range and extends the operation range.

The principle operation of the proposed converter is represented in Section II. The relevant analysis is given in Section III. Finally, a 1kW prototype of the proposed converter is implemented to confirm its theoretical analysis and validity.

II. PRINCIPLE OPERATION OF THE PROPOSED CONVERTER

Fig.1 shows a circuit diagram of the proposed converter. On the primary side of the power transformer T , the proposed converter has a FB circuit with one blocking diode DB and one clamp capacitor C_c . On the secondary side, there is a voltage doubler rectifier. The operation of the proposed converter can be classified into two cases. The one is a PSFB series-resonant converter mode and the other is an active-clamp step-up converter mode.

To analyze the steady-state operation of the proposed converter, several assumptions are made

- 1) All switches $S1$, $S2$, $S3$, and $S4$ are considered as ideal switches except for their body diodes and output capacitors.

- 2) The clamp capacitor C_c and output capacitor C_o are large enough, so the clamp capacitor voltage V_c and output voltage V_o have no ripple voltage, respectively.
- 3) The transformer T is composed of an ideal transformer with the primary winding turns N_p , the secondary winding turns N_s , the magnetizing inductance L_m , and the leakage inductance L_{lk} .
- 4) The capacitance of the resonant capacitors C_{r1} and C_{r2} is identical. Thus, $C_{r1} = C_{r2}$.

A. PSFB Series-resonant Converter Mode

Under the normal input voltage range, the proposed converter is operated by phase-shift control. In this mode, V_c is the same as the input voltage V_d and D_B is conducted. All switches are driven with a constant duty ratio 0.5 and short dead time. Fig. 2 and 3 show the operation waveforms and equivalent circuits, respectively. A detailed mode analysis is given as four modes.

Mode 1 [t_0, t_1]: Prior to t_0 , the switches S_1 and S_2 are in on state and the secondary current i_s is zero. The primary current i_p flows through D_B , S_1 , S_2 , and L_m . During this mode, the primary voltage v_p and secondary voltage v_s of the transformer T are zero. Thus, the magnetizing current i_m is constant and satisfies as follows:

$$L_{ik} \frac{di_s(t)}{dt} = nV_d - v_{cr1}(t) \quad (2)$$

$$i_s(t) = C_{r1} \frac{dv_{cr1}(t)}{dt} - C_{r2} \frac{dv_{cr2}(t)}{dt} \quad (3)$$

Where v_{cr1} and v_{cr2} are the voltages across C_{r1} and C_{r2} , respectively. Since V_o is constant, the secondary current i_s can be obtained as

$$\dot{i}_s(t) = C_{r1} \frac{dv_{cr1}(t)}{dt} - C_{r2} \frac{d(V_o - v_{cr1}(t))}{dt} = C_r \frac{dv_{cr1}(t)}{dt} \quad (4)$$

Where the equivalent resonant capacitance C_r is $C_{r1} + C_{r2}$. Using Eqns. (2) and (4), the secondary current i_s can be calculated as

$$i_s(t) = \frac{nV_d - v_{cr1}(t_2)}{Z_r} \sin \omega_r(t - t_2) \quad (5)$$

$$i_m(t) = i_p(t) = i_m(t_0) \quad (1)$$

Mode 2 [t_1, t_2]: At t_1 , S_2 is turned off. Because i_p flowing through S_2 is very low, S_2 is turned off with near zero-current. In this mode, i_p charges C_{S2} and discharges C_{S4} .

Mode 3 [t_2, t_3]: At t_2 , the voltage across S_4 reaches zero. At the same time, i_p flows through the body diode DS_4 . Thus, S_4 is turned on with zero-voltage while DS_4 is conducted. In this mode, v_s is nV_d where the turn ratio n of the transformer is given by N_s/N_p and the secondary current i_s begins to flow through $D1$. The state equation of this mode is written as follows:

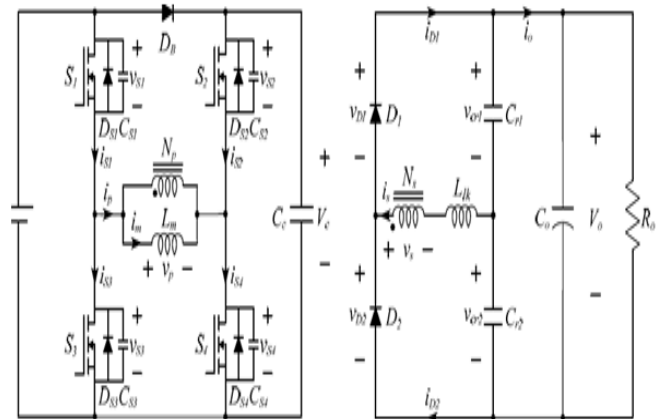


Fig. 1. Circuit diagram of the proposed hybrid-type full-bridge dc/dc converter.

The angular frequency ω_r and characteristic impedance Z_r are given by

$$\omega_r = \frac{1}{\sqrt{L_{lk} C_r}}, \quad Z_r = \sqrt{\frac{L_{lk}}{C_r}} \quad (6)$$

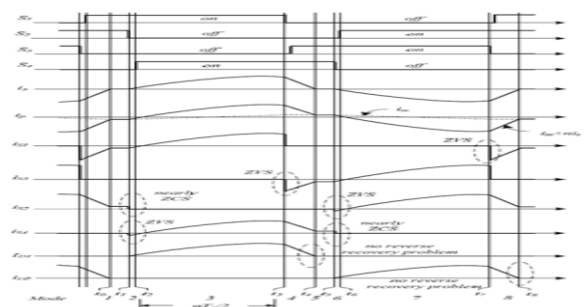


Fig. 2. Operation waveforms in the PSFB series-resonant converter mode.

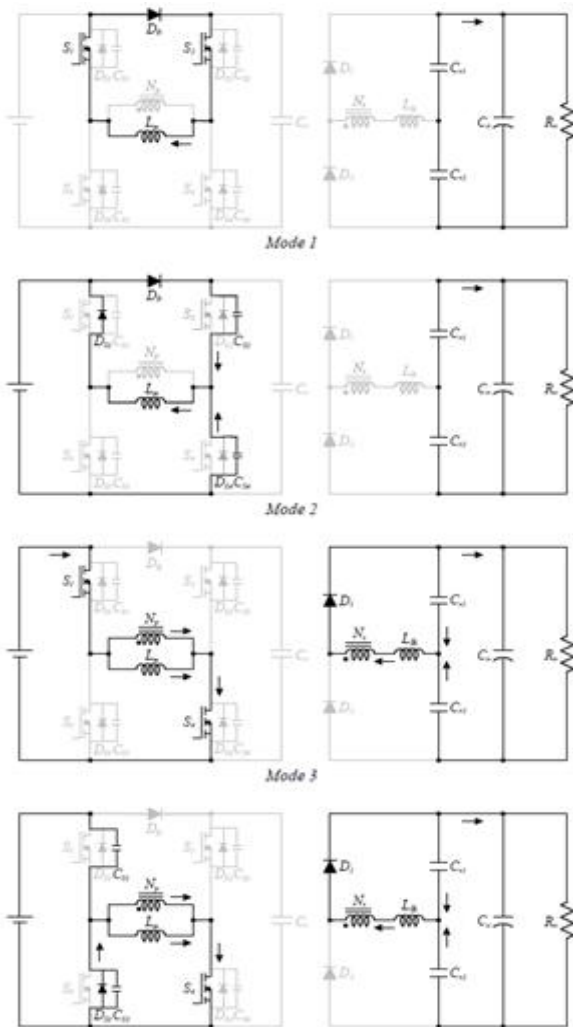


Fig. 3. Equivalent circuits during half period in the PSFB series-resonant converter mode

Mode 4 [t_3, t_4]: This mode begins when S_1 is turned off. The primary current i_p charges C_{S1} and discharges C_{S3} . When the voltage across S_3 becomes zero, i_p flows through the body diode D_{S3} . Thus, S_3 is turned on with zero-voltage while D_{S3} is conducted. When v_{p1} is zero, D_1 is still conducted and $-v_{cr1}$ is applied to L_r . Thus, the secondary current i_s goes to zero rapidly. End of this mode, since the secondary current is close to zero before D_1 is reverse biased; the losses by the reverse recovery problem are small as negligible. Since operations during the next half switching period are similar with *Mode 1-4*, explanations of *Mode 5-8* are not presented.

B. Active-clamp Step-up Converter Mode

As the information voltage diminishes up to a specific least estimation of the typical information go, the stage shift esteem ϕ increments up to its most extreme quality, 1. On the off chance that the information voltage is lower than the base estimation of the ordinary information run, the proposed converter is worked by double unbalanced heartbeat width tweak (PWM) control. The switches (S_1, S_4) and (S_2, S_3) are dealt with as switch matches and worked correlatively with short dead time. The obligation D more than 0.5 depends on (S_1, S_4) pair. In this circumstance, the brace capacitor voltage V_c is higher than V_d . At that point, the blocking diode D_B is opposite one-sided and the proposed converter works as the dynamic clasp venture up converter. Fig. 4 and 5 demonstrate the operation waveforms and identical circuits in the dynamic clip venture up converter mode, separately.

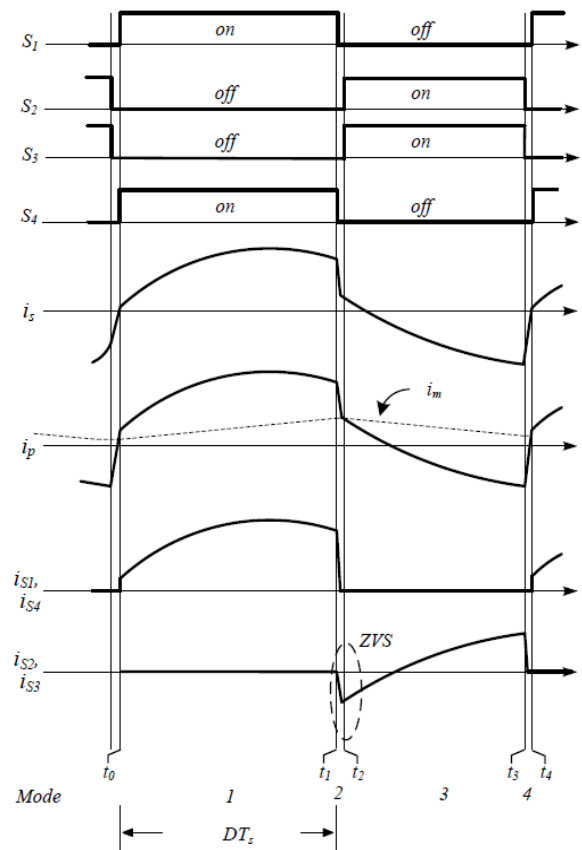


Fig. 4. Operation waveforms in the active-clamp step-up converter mode

Mode 1 [t_0, t_1]: At t_0 , S_1 and S_4 are turned on. Since V_d is applied to L_m , the magnetizing current i_m is linearly increased and is expressed as

$$i_m(t) = i_m(t_0) + \frac{V_d}{L_m}(t - t_0) \quad (8)$$

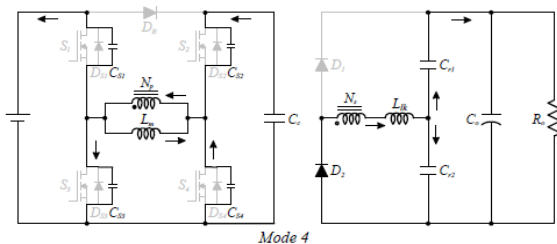
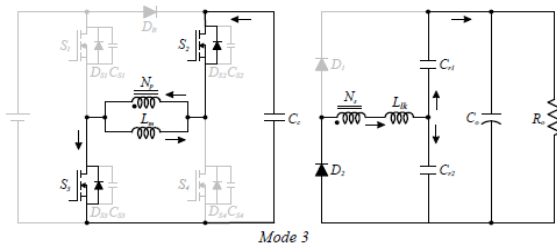
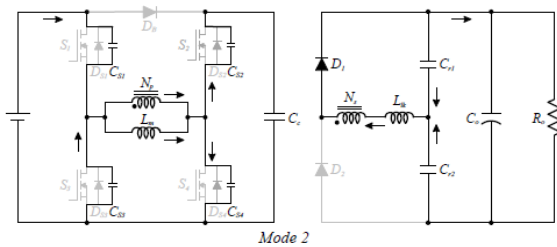
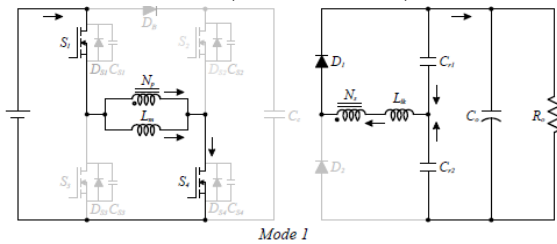


Fig. 5. Equivalent circuits during a switching period in the active-clamp step-up converter mode.

D_1 is conducted and the secondary current i_s begins to resonate by L_{lk} , C_{r1} , and C_{r2} . In this mode, the state equation is written as follows:

$$L_{lk} \frac{di_s(t)}{dt} = nV_d - v_{cr1}(t) \quad (9)$$

$$i_s(t) = C_{r1} \frac{dv_{cr1}(t)}{dt} - C_{r2} \frac{dv_{cr2}(t)}{dt} = C_r \frac{dv_{cr1}(t)}{dt} \quad (10)$$

From Eqns. (9) and (10), the secondary current i_s can be calculated as

$$i_s(t) = i_s(t_3) \cos \omega_r(t - t_3) - \frac{nV_c - v_{cr2}(t_3)}{Z_r} \sin \omega_r(t - t_3) \quad (11)$$

In this mode, power is transferred from the input to the output.

Mode 2 [t_1, t_2]: At t_1 , S_1 and S_4 are turned off. The primary current i_p charges and discharges the output capacitors of the switches during very short time.

Mode 3 [t_2, t_3]: This mode begins when the voltages across S_2 and S_3 are zero. At the same time, i_p flows through DS_2 and DS_3 . Thus, S_2 and S_3 are turned on with zero-voltage. Since the negative voltage $-V_c$ is applied to L_m , the magnetizing current i_m decreases linearly as

$$i_m(t) = i_m(t_3) - \frac{V_c}{L_m}(t - t_3) \quad (12)$$

In this mode, the secondary current i_s begins to second resonance and the state equation is written as follows:

$$L_{lk} \frac{di_s}{dt} = v_{cr2}(t) - nV_c \quad (13)$$

$$i_s(t) = C_{r1} \frac{dv_{cr1}(t)}{dt} - C_{r2} \frac{dv_{cr2}(t)}{dt} = C_r \frac{dv_{cr2}(t)}{dt} \quad (14)$$

Using Eqns. (13) and (14), the secondary current is given by

$$i_s(t) = i_s(t_3) \cos \omega_r(t - t_3) - \frac{nV_c - v_{cr2}(t_3)}{Z_r} \sin \omega_r(t - t_3) \quad (15)$$

Mode 4 [t_3, t_4]: At t_3 , S_2 and S_3 are turned off. The primary current i_p charges CS_2 , CS_3 and discharges CS_1 , CS_4 during very short time.

III. ANALYSIS OF THE PROPOSED CONVERTER

In the PSFB series-resonant converter mode, *Mode 4* is neglected since the duration of *Mode 4* is relatively very short. During *Mode 3*, the secondary current i_s in Eqn. (5) flows through D_1 ; the current is the same as sum of the current charging C_{r1} and current

discharging $Cr2$. As shown in Fig.3, during the half switching period $T_s/2$, $Cr2$ is discharged as much as the load current i_o while $Cr1$ is charged. Thus, the average value of the current flowing through $D1$ is the same as twice the load current during $T_s/2$. Due to the symmetric operation, the average value of the current flowing through $D2$ is also twice the load current during the next half switching period. Both average values of v_{cr1} and v_{cr2} are $V_o/2$ and $v_{cr1}(t_2)$ in Eqn. (5) is obtained from the ripple voltage Δv_{cr1} of $Cr1$ as

$$v_{cr1}(t_2) = \frac{V_o}{2} - \frac{\Delta v_{cr1}}{2} = \frac{V_o}{2} - \frac{1}{2C_{r1}} \int i_{cr1}(\tau) d\tau$$

$$= \frac{V_o}{2} \left(1 - \frac{T_s}{2C_{r1}R_o} \right) = \frac{V_o}{2} \left(1 - \frac{\pi Q}{2F} \right) \quad (16)$$

Where the frequency ratio F and quality factor Q are given by

$$f = \frac{f_s}{f_r}, Q = \frac{4\omega_r L_{lk}}{R_o} = \frac{4}{\omega_r C_r R_o} \quad (17)$$

Because the average value of the current flowing through $D1$ during $T_s/2$ is the same as $2i_o$ and is zero during next half switching period, the average value of the current flowing through $D1$ during T_s is equal to i_o . Thus, the load current i_o can be derived as

$$i_o = \frac{V_o}{R_o} = \frac{1}{T_s} \left[\int_{t_1}^{t_1+\varphi T_s/2} \frac{nV_d - v_{cr1}(t_2)}{Z_r} \sin \omega_r(\tau - t_2) d\tau \right]$$

$$= F \left[\frac{nV_d - v_{cr1}(t_2)}{2\pi Z_r} (1 - \cos \frac{\pi\varphi}{F}) \right] \quad (18)$$

From Eqns. (16) and (18), the voltage gain in the PSFB series-resonant converter mode can be derived as follows:

$$\frac{V_o}{V_d} = \frac{2n}{\frac{\pi Q}{F(1 - \cos \frac{\pi\varphi}{F})} + \left(1 - \frac{\pi Q}{2F} \right)} \quad (19)$$

Fig. 6 shows the normalized voltage gain in the PSFB series-resonant converter mode. In the active-clamp step-up converter mode, the average voltage V_c for $D > 0.5$ is obtained as:

$$V_c = \frac{D}{D-1} V_d \quad (20)$$

By the volt- second balance law for the magnetizing inductance L_m , the following equations are derived as

$$nV_d D T_s = \frac{n^2 L_m}{n^2 L_m + L_{lk}} V_{cr2} (1-D) T_s \quad (21)$$

$$\frac{n^2 L_m}{n^2 L_m + L_{lk}} V_{cr1} D T_s = nV_c (1-D) T_s \quad (22)$$

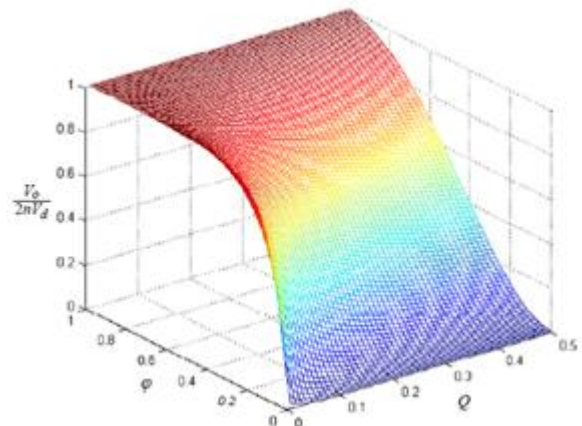


Fig. 6. Normalized voltage gain at $F=1.05$ in the PSFB series-resonant converter mode.

Where V_{cr1} and V_{cr2} are the average values of the voltages across C_{cr1} and C_{cr2} , respectively. The sum of V_{cr1} and V_{cr2} is V_o . From Eqns. (21) and (22), the average values V_{cr1} and V_{cr2} are obtained as

$$V_{cr1} = \frac{n^2 L_m + L_{lk}}{nL_m} V_d = (1-D)V_o \quad (23)$$

$$V_{cr2} = \frac{n^2 L_m + L_{lk}}{nL_m} \frac{D}{1-D} V_d = DV_o \quad (24)$$

Assuming L_{lk} is much smaller than L_m , the voltage gain in the active-clamp step-up converter mode can be derived as follows:

$$\frac{V_o}{V_d} = \frac{n}{1-D} \quad (25)$$

The voltage gain becomes that of an isolated boost converter. It means that the proposed converter performs step-up function in the active-clamp step-up converter mode.

In the PSFB series-resonant converter, the leading-leg switches $S1$ and $S3$ can be easily turned on with zero-voltage by the reflected secondary current. However, when the state of the lagging-leg switches $S2$ and $S4$

are changed, the secondary current is zero. Thus, only the energy stored in L_m is involved in ZVS of the lagging-leg switches condition; it is obtained as

$$\frac{1}{2}L_m\left(\frac{\Delta i_m}{2}\right)^2 = \frac{1}{2}L_m\left(\frac{\phi V_d}{4L_m f_s}\right)^2 > \frac{4}{3}C_m V_d^2 \quad (26)$$

Where C_m is the output capacitance of the MOSFET switches. From Eqn. (26), the magnetizing inductance L_m can be decided as

$$L_m < \frac{3\phi_{min}^2}{128C_m f_s^2} \quad (27)$$

Where ϕ_{min} is the minimum value of ϕ . The ZCS condition of the lagging-leg switches is related to the frequency ratio. As F increases, the ZCS range decreases [15]. Therefore, to guarantee both ZVS of all primary switches and ZCS of the lagging-leg switches, F should be selected to be slightly more than one. In the active-clamp step-up converter mode, S_2 and S_3 can achieve ZVS turn-on naturally from the asymmetrical PWM operation.

As shown in Fig.2, in the PSFB series-resonant converter mode, L_{lk} performs as the output inductor and all energy stored in L_{lk} is delivered to the load until the secondary current is zero. Then, only small magnetizing current flows on the primary side. In the active-clamp step-up converter, the proposed converter is operated by dual asymmetrical PWM control scheme. In the PWM scheme, there is no circulating current [22]. Thus, the proposed converter eliminates the conduction loss by the circulating current in the entire operation range.

IV. IMPLEMENTATION AND EXPERIMENTS

To evaluate a feasibility of the proposed converter, a 1kW prototype was built and tested. The operation range of the proposed converter is from 250V to 350V. The output voltage is designated as 200V and the normal input range is set up from 320V to 350V

A. Implementation of The Prototype

Considering power conversion efficiency under the normal input range, the proposed converter is designed. To obtain ZVS turn-on of the switches, the switching frequency f_s should be higher than the

resonant frequency f_r . By the design rule proved in [15], the frequency ratio F (f_s/f_r) is selected to be slightly more than one. The quality factor Q is decided by Eqn. (17). If Q is too small, the proposed converter is operated with small ϕ under the normal input range. Thus, L_{lk} is selected as 8.3μH. From the normal input range, the turn ratio n is decided by Eqn. (19) and Fig. 6.

TABLE I: PARAMETERS OF THE PROTOTYPE

Parameters	Symbols	Value
Input voltage	V_d	250-350V
Output voltage	V_o	200V
Switching frequency	f_s	50kHz
Primary winding turns	N_p	24turns
Secondary winding turns	N_s	8turns
Magnetizing inductance	L_m	695μH
Leakage inductance	L_{lk}	8.3μH
Clamp capacitor	C_c	11μF
Resonant capacitors	C_{r1}, C_{r2}	680nF
Output capacitor	C_o	680μF
Switches	S_1, S_2, S_3, S_4	STW26NM60
Blocking diode	D_B	FFAF40U60DN
Output diodes	D_1, D_2	FFPF15U40S

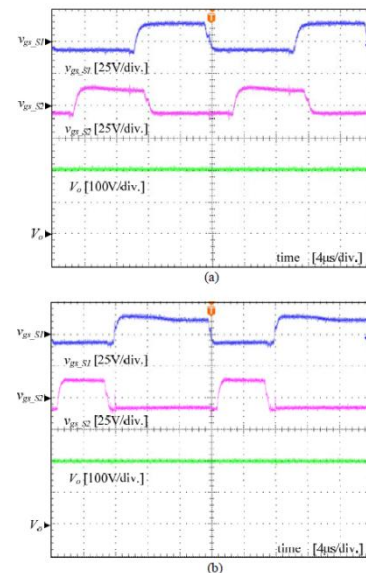


Fig. 7. Experimental waveforms for the gate signals and output voltage according to the operation mode. (a) PSFB series-resonant converter mode when $V_d = 350V$. (b) Active-clamp step-up converter when $V_d = 250V$

All switch stresses are determined by the input voltage in the PSFB series-resonant converter mode. On the other hand, in the active-clamp step-up converter mode, the voltage stress of the switches $S1$ and $S2$ are the same as the input voltage and those of $S3$ and $S4$ are determined by Eqn. (20). In both the operation modes, voltage stresses of the rectifier diodes are clamped at the output voltage V_o . The major experimental parameters are presented in Table I. The prototype is implemented using a single DSP chip, dsPIC33EP512GM604 (Microchip) which provides both phase-shift and asymmetrical PWM control.

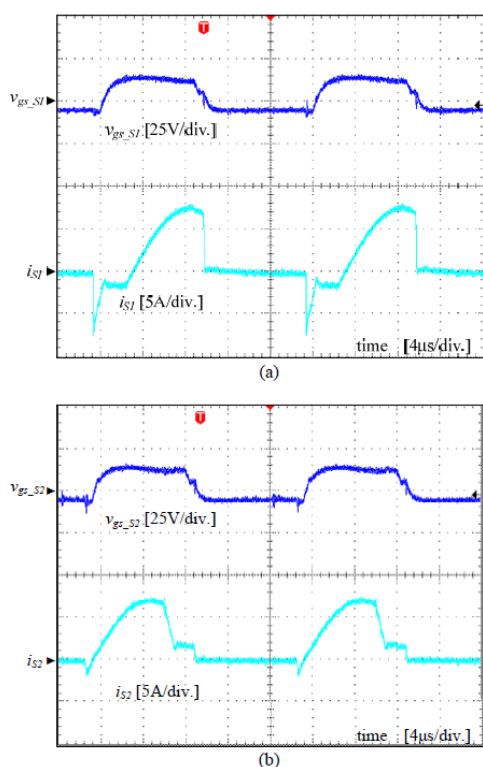


Fig. 8. Experimental waveforms for soft switching in the PSFB series-resonant converter mode. (a) ZVS turn-on of S1. (b) ZVS turn-on and ZCS turn-off of S2.

B. Experimental Results

Fig. 7 indicates waveforms for the door flags and yield voltage in the proposed converter as indicated by the operation mode. v_{gs_S1} and v_{gs_S2} are every door signal for $S1$ and $S2$, separately. At the point when the information voltage is 350V, the proposed converter is worked by stage shift control with the consistent

obligation 0.5. Then again, when the info voltage is 250V, the proposed converter is worked by the unbalanced PWM control with the obligation 0.61. In both operation modes, the proposed converter controls v_o . Fig. 8 (an) and (b) show waveforms for the entryway signs and streams of $S1$ and $S2$ at full load condition when $V_d = 350V$. At the point when the switches are turned on, the streams move through the body diode of every switch. Plainly all switches are turned on with zero-voltage. Besides, as appeared in Fig. 8 (b), $S2$ is killed with close to zero present as the hypothetical investigation. Fig. 9 show waveforms for the essential voltage v_p and current i_p of the ordinary PSFB arrangement thunderous converter and the proposed converter at full-stack condition under the typical information range. In the routine PSFB arrangement resounding converter, to ensure the assigned operation range, higher turn proportion n ($=0.417$) is required than the proposed converter. Different parameters are appeared in Table I. At the point when the info voltage V_d is 350V, the routine converter works with little ρ ($=0.5$).

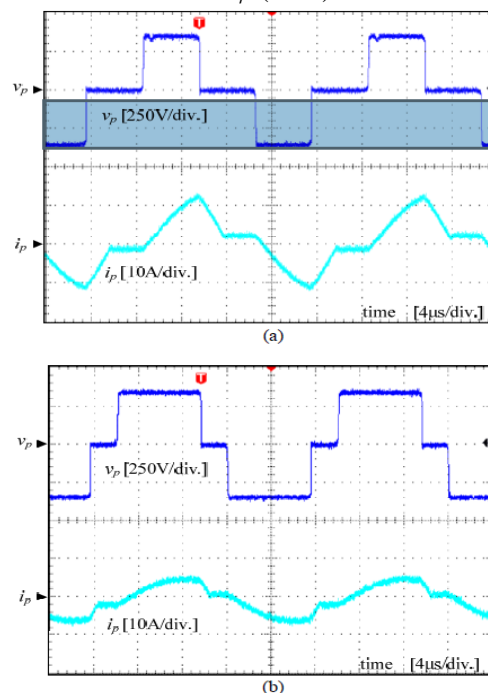


Fig. 9. Experimental waveforms for the current stress when $V_d = 350V$. (a) Conventional PSFB series-resonant converter. (b) Proposed converter.

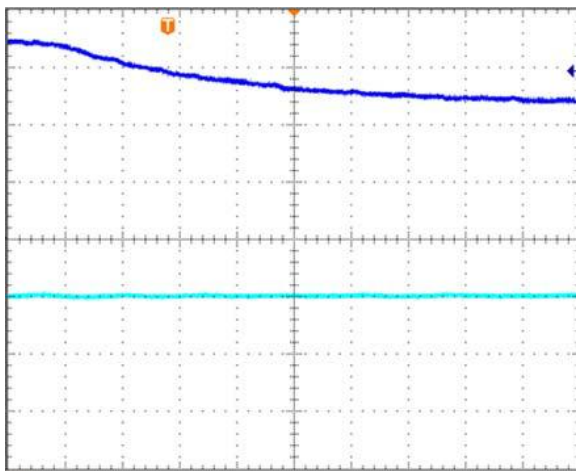


Fig. 10. Experimental waveforms for the input voltage V_d and output voltage V_o in the transition-state.

Then again, the proposed converter is worked with bigger ϕ ($=0.75$). As appeared in Fig. 9, the present anxiety in the proposed converter is much lower. What's more, the proposed converter dispenses with the coursing current. Fig. 10 demonstrates waveforms for the information and yield voltages in the transient-state. At the point when the information voltage V_d is decreased from 350V to 250V, the proposed converter manages the yield voltage with no hysteresis. Fig. 11 demonstrates measured efficiencies for the routine arrangement thunderous converter and the proposed converter when $V_d = 350V$. It demonstrates that the proposed converter has higher productivity over all heap conditions. Fig. 12 demonstrates the variety of the yield voltage V_o at full-stack condition when the information voltage V_d diminishes from 250V to 200V.

As appeared in Fig. 12, in the underneath assigned operation scope of the ordinary converter, V_o diminishes. In the proposed converter, V_o is kept up as 200V in spite of the fact that the info voltage diminishes underneath the assigned operation range. Fig. 13 demonstrates the similar plot of investigative and trial voltage addition of the proposed converter. At the point when the stage shift esteem ϕ is communicated utilizing the obligation D , $\phi/2$ can be spoken to as D . The deliberate voltage addition is like

the hypothetical examination in Eqns. (19) and (25). As appeared in the Fig. 13, the proposed converter has both the progression down and venture up capacities.

V. CONCLUSION

The novel crossover sort full-connect dc/dc converter with high productivity has been presented and confirmed by the investigation and exploratory results. By utilizing the half and half control plan with the straightforward circuit structure, the proposed converter has both the progression down and venture up capacities, which guarantee to cover the wide information range. Under the ordinary information run, the proposed converter accomplishes high productivity by giving delicate changing method to all the switches and rectifier diodes, and decreasing the present anxiety.

At the point when the information is lower than the ordinary information go, the proposed converter gives the progression up capacity by utilizing the dynamic clip circuit and voltage doubler, which augments the operation range. To affirm the legitimacy of the proposed converter, 1kW model was constructed and tried. Under the ordinary information extend, the transformation effectiveness is more than 96% at full-stack condition, and the information range from 250V to 350V is ensured. Along these lines, the proposed converter has numerous favorable circumstances, for example, high effectiveness and wide information range.

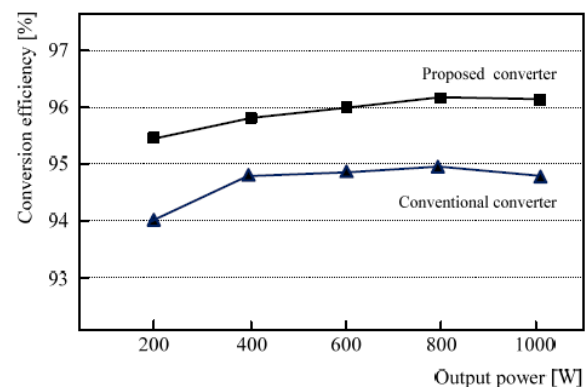


Fig. 11. Measured efficiencies under the normal input range according to the output power

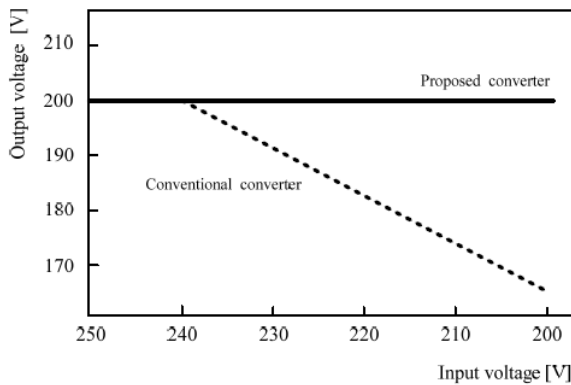


Fig. 12. Variation of output voltage in the below designated operation range

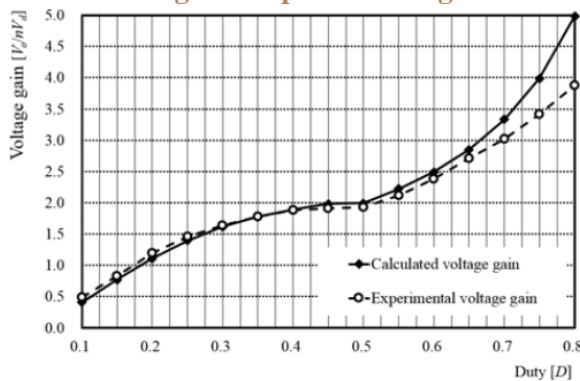


Fig. 13. Comparison between analytical and experimental voltage gain

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