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A Novel Design of Reversible Binary and BCD Adders using Verilog HDL

Koppera Manasa
M.Tech (VLSISD),
Anurag Engineering College.

Dr.N.V.N.Ravi Kumar
M.Tech, Ph.D, MISTE, Professor,
Department of ECE,
Anurag Engineering College.

M.Basha, M.Tech
Associate Professor & HOD
Department of ECE,
Anurag Engineering College.

Abstract:

Programmable reversible logic design is trending as a prospective logic design style for implementation in recent nanotechnology and quantum computing with low impact on circuit heat generation. Reversible logic has emerged as a possible low cost alternative to conventional logic in terms of speed, power consumption and computing capability. An adder block is a very basic and essential component for any processor and optimized design of these adders' results in efficient processors. In this work we propose optimized Binary adders and BCD adders. The adders designed in this work are optimized for Quantum cost, Delay and Area. A modified BCD adder is also proposed which removes redundancy in the circuit and acts as most efficient BCD adder. Here we explore the use of Negative control lines for detecting overflow logic of BCD adder which considerably reduces Quantum cost, delay and gate count which result in high speed BCD adder with optimized area which give way to lot of scope in the field of reversible computing in near future.

Keywords: Negative controlled Toffoli, Binary adder, BCD adder, Quantum cost.

I. INTRODUCTION

Classical computing devices process large amount of digital data using logical (Boolean) operations. A single bit of information is erased after every logical operation. Landauer proposed that KT ln(2) joules of energy are lost for erasing a single bit of data, where K is the Boltzmann's constant and T is the absolute temperature at which computation is performed [18].

A circuit is said to be reversible if for each input there exists a unique output i.e., number of inputs must be equal to number of outputs An operation is said to be physically reversible if it converts no energy to heat and produces no entropy [3]. A logic circuit is said to be reversible if it computes a bijective (one-to-one and onto) logic functions [4]. A reversible circuit has neither feedback nor fan-out allowed [5]. In any digital system, adder block is the most essential one. Ripple carry adder and BCD adder are very commonly used in digital systems. Reversible BCD adders have large applications in quantum computing, electronic display systems, real time clock implementation in PC's and also in floating point algorithm implementation. In the present day scenario, technology scaling is believed to be at its greater heights and further scaling leads to lots ofcomplexities. Hence, there is a need for a low power circuitswith optimized area.

Reversible logic is one of the solution forthe above problem which is emerging as a low poweralternative for conventional logic. Among the reversible gates, n*n Toffoli is very commonly used reversible gate in digitalcircuits with positive control lines. In this work, we explorethe use of negative controlled Toffoli gate to implement theoverflow logic of BCD adder. Incorporating negative controllines leads to smaller circuits with respect to the number ofgates i.e., reduction with respect to gate count as well asquantum cost and the run-time of the synthesis can be improved [6, 7]. In this paper, we have designed a I-bit reversible binary full adder using Toffoli gates with zero garbage output andhave extended the same to realize 4-bit reversible binary fulladder with optimized Quantum cost compared to previous works.

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In addition to that, a reversible BCD adder design hasbeen proposed with Quantum cost much lesser than theprevious work using negative controlled Toffoli gates and proposed binary full adder circuit.Also, a modified BCD adderis proposed which removes redundancy in the proposed circuitand is optimized in all aspects.

II. LITERATURE SURVEY:

Design of combinational block using the concept of negative control lines is an emerging trend in VLSI domain. This is because of its capability of replacing series of gates and thereby reducing the area, gate count and as well as power consumption. Various synthesis and design techniques have been proposed using negative control lines. [6] proposes a post-synthesis DD based optimization technique using negative control lines. Exact synthesis algorithms give minimal circuit for a given function. Negative control lines are used in [7] to optimize this algorithm. But computational time is large and applicable only to small functions. Optimization based on template matching technique is another method proposed in [9] which defines set of rules to efficiently replace NCT in place of series of PCT, thus reducing gate count, area and power consumption. [10] proposes a reversible binary and BCD adder circuit with optimized ancilla inputs and garbage outputs.

Design of reversible binary and BCD adders have been proposed in [15] with a goal of optimizing number of ancilla input bits and the garbage outputs. [13] proposes a modular synthesis method to realize a reversible BCD adder circuit. But delay of the circuit is not taken into account. In [17] BCD adder has been designed using New gates and FG gates. They have considered only the garbage outputs. Quantum cost, delay and ancilla inputs have not been discussed. Another BCD adder design has been proposed in [15] using five HNG gates, one Peres gate, one Feynman gate and one SCL gate. They have also not considered quantum cost into account. In this paper, we have proposed a new I-bit reversible adder with optimized quantum cost consisting of only Toffoli gates.

A 4-bit binary full adder and BCD adder is realized using the proposed I-bit binary full adder. The proposed BCD adder is then modified to remove redundancy in the circuit which makes it more efficient in terms of area and delay. Different parameters which characterizes any reversible circuits such as quantum cost, delay, ancilla inputs and garbage outputs has been considered and compared with the existing designs. All the designs have been generalized to n-bits and compared with the previous works.

III. REVERSIBLE GATES:

A reversible gate is an n-input and n-output (denoted by n × n) gate that produces a unique output pattern for each possible input pattern. In other words, reversible gates are circuits in which the number of outputs is equal to the number of inputs and there is a one-to-one correspondence between the vectors of inputs and outputs. Feynman gate is a 2*2 one through reversible gate as shown in figure 2.1. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=A⊕B. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs.

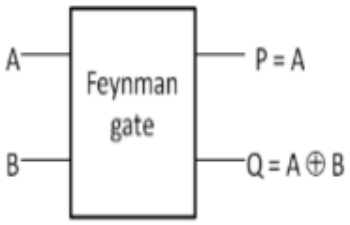

Fig. 1: Feynman gate

The 3*3 Toffoli gate has the input vector I (A, B, C) and the output vector isO(P,Q,R). The outputs are defined by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5.

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Fig. 2: Positive Controlled Toffoli gate (TG) b: TG Symbol

A negative controlled Toffoli gate has one or more negative control lines. In this case toggling happens at target bit if all negative control lines are at logic 0 and if any positive control, it should be at logic I. The Quantum Cost of Negative controlled Toffoli gate is 6 with a delay of M. A 3- bit negative controlled Toffoli is as shown in Fig 3.

Fig. 3: Negative controlled Toffoli (NCT) gate b: NCT symbol

IV. PROPOSED DESIGN

A. I-bit Reversible Full Adder

There are various variants of Toffoli gate. 2*2 Toffoli gate is generally called CNOT gate / Feynman gate.A I-bit reversible full adder has been designed using only n*n positive controlled Toffoli gates as shown in Fig 4. The proposed design is simple and has a gate count of 4 with 0 garbage output.

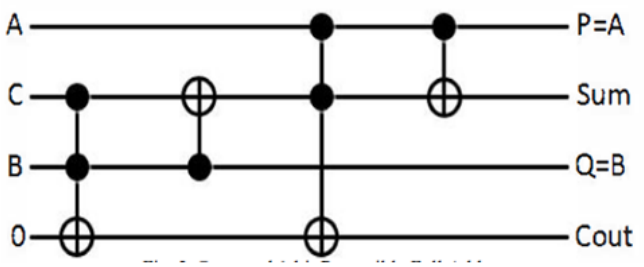

Fig. 4. Proposed I-bit Reversible Full Adder

B. 4-bit Reversible Full Adder

Proposed reversible 4-bit ripple carry adder has been designed using four I-bit reversible adders as shown in Fig 5. It is characterized by a quantum cost of 48 and a delay of 40t:J.. For each stage of input, I ancilla input is required producing no garbage output. The proposed design performs better in terms of quantum cost and delay when compared to previous works. When compared to [15, 19], the quantum cost has been reduced by 18.75% for an 8-bit adder. In rest of the paper proposed reversible 4-bit full adder will be called by the name 'NAFA'.

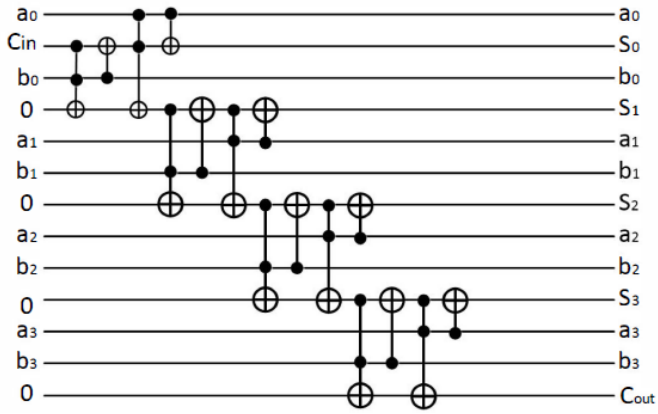

Fig. 5. Proposed 4-bit Reversible Full Adder Design (NAF A)

C. 4-bit Reversible BCD Adder Design (Design 1)

BCD codes makes calculation and analysis more simple in processor design. A BCD adder plays a major role in these designs. A conventional BCD adders are constructed using Full Adder circuit with an overflowing detector circuit. In this design we have proposed a 4-bit reversible BCD adder using proposed reversible full adder circuit (NAF A) and an overflow detector circuit as shown in Fig 6. The overflowing detector circuit has been designed using two 3 *3 negative controlled Toffoli gates and a positive controlled Toffoli gate. The use of negative logic reduces the gate count and hence aids the requirement. In this design two reversible 4-bit full adders (NAF A) are used to realize the reversible BCD adder.

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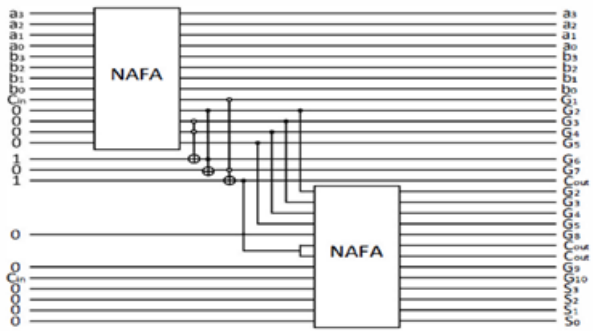

Fig 6: Proposed 4-bit Reversible BCD adder design

D.Modified 4-bit Reversible BCD Adder Design (Design 2):

A BCD code consists of numbers from 0 to 9 and any value greater than the range is corrected by adding 6 (0 I 10) to the resulting value. There is a need to detect this overflow of the resulting value. Hence we have designed overflow logic using negative controlled Toffoli gate followed by a 4-bit reversible full adder to add 6 to the resulting value. But we need to add l's only for 2nd and 3rd bits. Hence we need only two I-bit adders to perform the same instead of 4-bit full adder as discussed in previous section. Hence we modified the previously proposed BCD adder design with the one as shown in Fig 7.

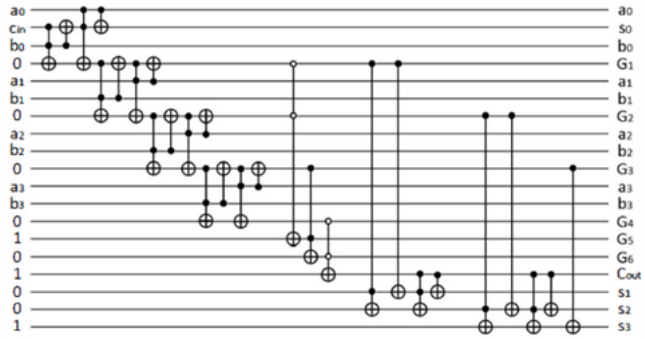

Fig 8: Proposed 4-bit Modified Reversible BCD Adder Design

IV.METHODOLOGY AND ANALYSIS

A. Reversible Binary Full Adder:

The methodology adapted is to ripple the carry through each stage of full adder circuit.

Thus the proposed 4-bit reversible full adder is the cascade of four I-bit full adders with a Quantum cost of 48 and delay of 40LL The delay calculation process has been shown diagrammatically in Fig 7. According to the design, for each group of 2*2 and 3*3 Toffoli gate, delay is found to be

$$\Delta = \max(1\Delta, 5\Delta) = 5\Delta$$

Since there are 8 such pairs, the total delay for a 4-bit reversible full adder is found to be 40Δ. the general expression to find delay for an n-bit reversible binary adder is as shown below:

$$\Delta_{\text{total}} = \sum_{i=1}^{2n} \max(1\Delta, 5\Delta)$$

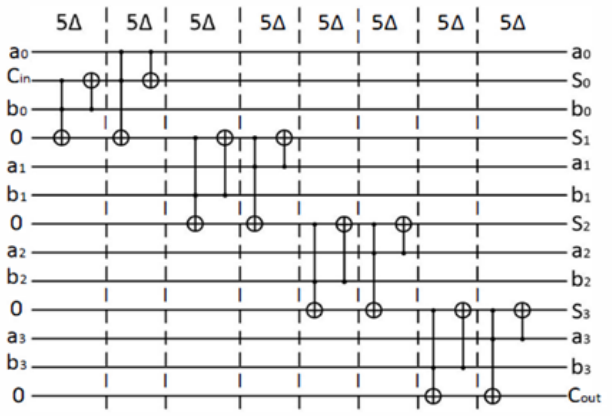

Fig 7: Delay Calculation in 4-bit Reversible Full Adder design

B.Reversible BCD Adder:

A binary coded decimal is a form of number system in which every four bits of a number is represented by its equivalent value. For example, a decimal number 45 is represented as 0100 0101 in BCD system. This makes things simple and facilitates the logic designer to understand the logic. While designing a combinational circuit using BCD logic, we may need to perform different operations on it such as addition, subtraction, etc. While performing any operation, there may be chances of overflowing the range of the number system. In such a case, a detector and corrector circuit needs to be present.

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During BCD addition if there is any overflow, the logic to correct is to add 6 (0 I I 0) to the resulting data. The design methodology involves detecting overflow of the resulting sum from 4-bit reversible full adder and then adding 6 to it using another 4-bit reversible full adder. In this proposed design, we have used cascade of two negative controlled Toffoli and a positive controlled Toffoli gate to detect the overflow and have used another 4-bit reversible binary adder to correct it by adding 6 (0110) to the output of first full adder. By this the quantum cost has been found to be 113 with gate count of 35 and delay of 97LL In case of modified full adder (Design 2), we have removed the redundancy present in the reversible BCD adder proposed (Design I) as we need only two I-bit full adder instead of 4-bit full adder. This will reduce the delay as well as area.

V.COMPARISION RESULTS

A. Reversible Binary Full Adder:

n-bit reversible binary full adder proposed is characterized by the quantum cost of 12n, delay of IOn, 4n ancilla inputs and 0 garbage outputs. When compared to [15, 19], the quantum cost of the proposed design has been reduced by 18.75% for an 8-bit adder. The delay has been improved by 7.5% when compared to [18]. Table I gives the comparison of n-bit full reversible binary full adder.

TABLE 1. COMPARISON OF N-BIT REVERSIBLE FULL ADDER

	Ancilla Inputs	*Garbage Outputs*	*Quantum Cost*	*Delay Δ*
[18]	0	0	17n-6	10n+6
[19]	0	0	17n-22	15n-6
[15]	0	0	15n-6	9n+1
Proposed	4n	0	12n	10n

B. Reversible BCD Adder:

TABLE II. COMPARISON OF 4-BIT REVERSIBLE BCD ADDER

	Ancilla Inputs	*Garbage Outputs*	*Quantum Cost*	*Delay Δ*
[10]	68	72	440	Not Mentioned
[11]	28	24	220	Not Mentioned
[12]	16	16	676	Not Mentioned
[13]	56	64	336	Not Mentioned
[14] (Design 3*)	8	24	412	Not Mentioned
[15] (Work 3*)	4	3	280	228
[16]	6	10	Not Mentioned	Not Mentioned
[17]	17	22	Not Mentioned	Not Mentioned
Proposed (Design 1)	13	10	113	97
Proposed (Design 2))	10	6	90	80

In [14] 6 designs and in [15],4 works on BCD adders are proposed based on varying parameters such as Ancilla inputs, garbage outputs, quantum cost and the delay. Among them, the design with minimum Ancilla inputs and garbage outputs are compared here.

VI.SIMULATION RESULTS:

The corresponding simulation results of the floating point adders are shown below. All the synthesis and simulation results are performed using Verilog HDL. The synthesis and simulation are performed on Xilinx ISE 14.4. The simulation results are shown below figures.

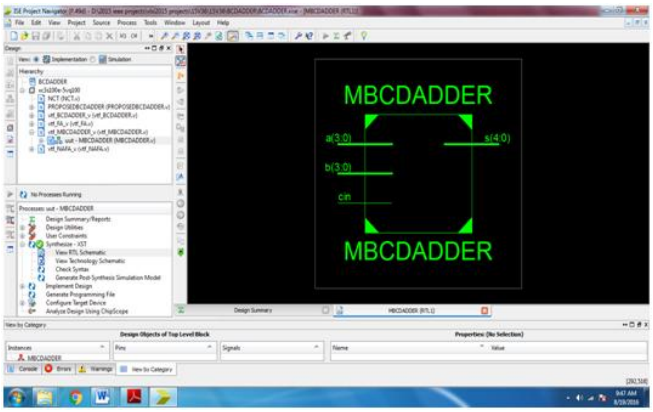

Figure-7: RTL schematic of Top-level of proposed 4-bit BCD adder

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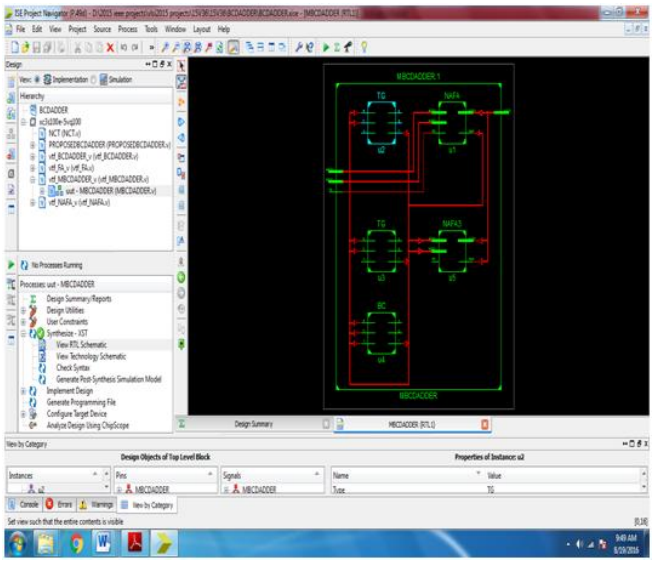

Figure 8: RTL schematic of Internal block of proposed 4-bit BCD adder

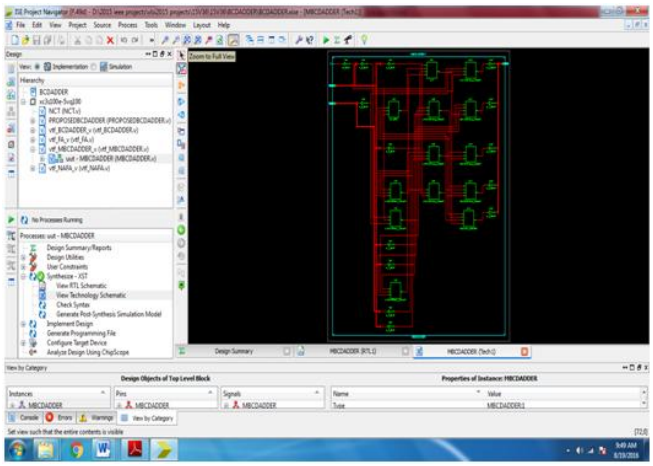

Figure 9: Technology schematic of proposed 4-bit BCD adder

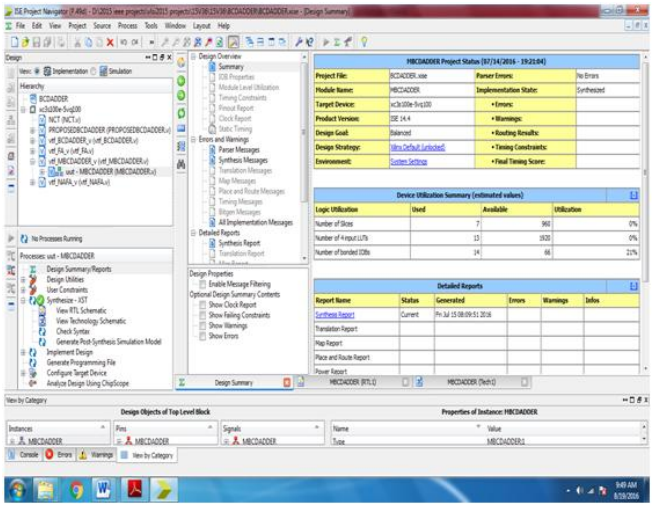

Figure 10: Synthesis report of proposed 4-bit BCD adder

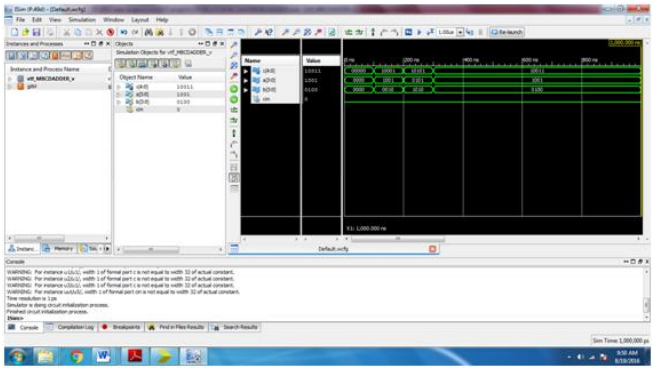

Figure 11: simulated outputs for proposed 4-bit BCD adder

VII.CONCLUSION AND FUTURE WORK

In this paper an optimized reversible BCD adder is presented. The design is very useful for the future computing techniques like ultra low power digital circuits and quantum computers. It is shown that the proposal is highly optimized in terms of number of reversible logic gates, number of garbage outputs and the delay involved. All the designs are functionally verified using Xilinx ISE14.4 tool. The use of negative control lines in the design for detecting overflow logic of BCD adder has considerably reduced delay and gate count which result in high speed BCD adder with optimized area. Thus we conclude that the use of Negative control lines reduces the gate count and hence area, for specific signal processing which gave way to lot of scope in the field of reversible computing in near future. The proposed reversible BCD adder can be used for designing large reversible systems, which is can be used in ultra low power digital circuits and quantum computers.

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