

Designing of High Speed Floating Point Unit Using Reversible Logic

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ABSTRACT

For count or representation of huge or small numbers, extensive territory is vital. These qualities can be spoken to utilizing the IEEE-754 standard based drifting point number juggling representation. The paper presents proficient methodology towards planning of rapid drifting point unit utilizing reversible rationale. Programmable reversible rationale outline is inclining as an imminent rationale plan style for execution in late nanotechnology and quantum figuring with low effect on circuit heat era. There are different reversible usage of sensible and number juggling units have been proposed in the current examination, however not very many reversible gliding point outlines has been composed. Skimming point operations are utilized much of the time as a part of about all figuring disciplines. The examination of proposed reversible circuit should be possible as far as quantum cost, rubbish yields, consistent inputs, power utilization, velocity and territory.

Keyword: Reversible logic, Garbage output, Quantum cost, Floating Point, Arithmetic Unit etc

INTRODUCTION

A number juggling circuit which performs computerized number-crunching operations has numerous applications in advanced co processors, application particular circuits, and so on. Due to the headways in the VLSI innovation, numerous intricate calculations that seemed unrealistic to put into practice have turned out to be effortlessly feasible today with wanted execution parameters so that new outlines can be fused. Present day PCs use traditions for speaking to non whole number numbers, the most broad of which is the IEEE 754 Standard for Floating-Point

computations. This standard characterizes parallel representation for gliding point quantities of fluctuating accuracy, giving particular case of the binary32 (or single exactness) configuration, binary64 (or twofold accuracy) organization, and it characterizes operations on coasting point numbers. The fundamental parts in IEEE 754 standard skimming point numbers are the sign, the example, and the mantissa.

Table I-Bit Range for Floating-Point Values

	Sign	Exponent	Fraction	Bias
Single precision	1(31)	8(30-23)	23(22-00)	127
Double precision	1(63)	11(62-52)	52(51-00)	1023

Table II-Floating Point Number Representation

32 Bit		
Sign	Exponent	Mantissa
1 bit	8 bit	23 bit

There are four sorts of exemptions that emerge amid gliding point operations. At whatever point the outcome can't be appeared as a distinct number in the accuracy organization of the goal the Overflow exemption is happened. The Underflow exemption happens when a middle result is little to be figured effectively. At the point when zero partitions a limited nonzero number, the Division by zero special case emerges. The Invalid operation special case is raised if the given inputs are not fitting for the operation to be performed. Reversible rationale is a promising registering outline worldview which exhibits a technique for developing PCs that create no warmth dispersal. Reversible figuring rose as a consequence of

the utilization of quantum mechanics standards towards the advancement of a general registering machine. The essential rule of reversible processing is that a bijective gadget with an indistinguishable number of information and yield lines will create a figuring situation where the electrodynamics of the framework take into consideration expectation of every single future state in view of known past states, and the framework achieves each conceivable state, bringing about no warmth dissemination. Reversible processing varies from routine figuring in that it plays out the calculation in a coherently reversible manner: The yield of a (completely) reversible circuit dependably particularly recognizes the information. Circuits can exploit this coherent reversibility to diminish power by reusing the data as opposed to disposing of it: Landauer demonstrated that at whatever time a touch of data is disposed of, it compares to some quantum of vitality lost as warmth [1]. Moreover in 1973, Bennett has demonstrated that this vitality misfortune can be decreased or even expelled if the circuits are composed utilizing reversible doors [2].

The rest of the paper is organized as takes after. Area II comprises of imperative points of interest of reversible rationale outline, with scope of some reversible rationale primitive entryways. Segment III gives subtle elements of gliding point expansion calculation and design. Segment IV traces approaches towards multiplier and divider plan. Segment V introduces our last estimations, a brief examination of the engineering, and heading for future work. Segment VI closes the paper with our rundown of references.

REVERSIBLE LOGIC PRIMITIVE

Numerous conventional rationale doors, for example, the AND, OR, NAND, NOR, and XOR entryways are on a very basic level irreversible. That is to say that the yield mix of any of these entryways does not uncover the information blend that brought about the yield. In this way we have a requirement for primitive reversible rationale entryways.

Reversible Gate

Reversible gates are the circuits having balanced relationship between vectors of info and yield. Consequently from yield vector state we can remake the vector of information states.

Quantum Cost

Each quantum circuit is fabricated utilizing 1X1 and 2X2 quantum primitives and its expense is computed as an aggregate total of 2X2 entryways utilized following 1X1 door has no expense, i.e., zero. Fundamentally the quantum primitives are framework operation which is connected on qubits state. Every one of the entryways of the structure 2X2 have measure up to quantum cost and the expense is solidarity, i.e., one [3]. Since each reversible door comprises of 1X1 or 2X2 quantum entryway, the quantum expense of a reversible configuration figures the aggregate number of 2X2 entryways utilized. The quantum expenses of Feynman door [4], Peres entryway [5] and DPG door (as full viper) [6] are one, four and six separately.

Garbage Output

Undesirable or unused yield of a reversible door (or circuit) is known as rubbish yield, i.e., the output(s) which is (are) required just to keep up the reversibility is(are) known as refuse yield (s).

Delay

The greatest number of doors in a course from any info signal line to any yield line is known as postponement of a circuit. Toward the starting, every door plays out the outline calculation in one unit time. Also, all inputs to the circuit are known before the calculation starts.

Popular Reversible Gate

1) Feynman Gate:

The input and output vectors of 2x2 Feynman Gate (FG) [4] are $(Ip)v$ and $(Op)v$ respectively and can be defined as follows:

$$(Ip)v = \{a\} \text{ and } (Op)v = \{a \text{ xor } b\}$$

2) Peres Gate:

The input and output vectors of 3x3 Peres Gate (PG) [5] are $(Ip)v$ and $(Op)v$ respectively and can be defined as follows:

$$(Ip)v = \{a,b,c\} \text{ and } (Op)v = \{a, a \oplus b, a \oplus b \oplus c\}$$

The 3 bit Peres gate has Quantum cost of 4.

3) Double Peres Gate-

Input vector, $(Ip)v$ and output vector, $(Op)v$ of 4x4 Double Peres Gate (DPG) [6] are defined as follows:
 $(Ip)v = \{a,b,c,d\}$ and $(Op)v = \{a, a \oplus b, a \oplus b \oplus d, (a \oplus b) \oplus d \oplus a \oplus b \oplus c\}$

4) Fredkin Gate

Input vector, $(Ip)v$ and output vector, $(Op)v$ of 3x3 Fredkin Gate (FR) are defined as follows:

$$(Ip)v = \{a,b,c\} \text{ and } (Op)v = \{a, a' \oplus b, a' \oplus c\}$$

5) HNG Gate

Input vector, $(Ip)v$ and output vector, $(Op)v$ of 4x4 HNG are defined as follows:
 $(Ip)v = \{a,b,c,d\}$ and $(Op)v = \{a, b, a \oplus b \oplus c, (a \oplus b) \oplus c \oplus a \oplus b \oplus d\}$

FLOATING POINT ADDITION

Given two drifting point numbers to be included, the IEEE754 Standard for Floating-Point Arithmetic subtle elements how their whole can be discovered [7]. First, if the types are not equivalent, the littler is increased until it adjusts to the bigger.

To adjust the skimming point number with the littler example without changing its esteem, its particular trailing signific and must be moved one spot to the ideal for each time the type is increased. Once the types are equivalent, the critical can be summed. The aggregate is then standardized and adjusted. Fig. 1 delineates the square level schematic of the engineering our proposed reversible gliding point snake plan employments.

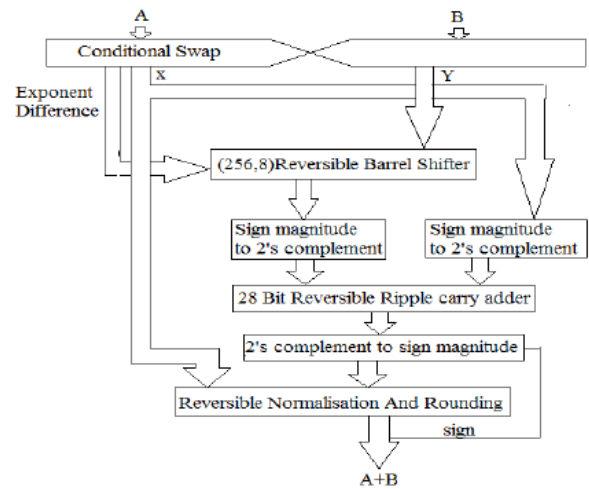


Fig-1 Proposed design of reversible addition architecture

Reversible Conditional Swapping

The initial phase in our reversible gliding pointer viper design is to swap the coasting point operands restrictively and reversibly. Whatever remains of the engineering works accepting that X is the coasting point number with the more noteworthy type, and Y is the skimming point number that conceivably should be adjusted to X. The examples of the two drifting point numbers both are unloaded and extended to nine bits. Keeping in mind the end goal to discover their distinction the exponent that is the minuend is supplemented utilizing two's supplemented, and with it the distinction is ascertained. The nine HNG entryways execute the reversible subtracter circuit [8]. The sign piece of the distinction of the examples goes about as the condition (control) by which the two whole gliding point numbers are swapped: If $expA < expB$, then the drifting point numbers will swap positions, generally $expA \geq expB$ and the coasting point numbers are gone through to the following stage without swapping.

Reversible Barrel Shifter

In our proposed framework we require (256,8) reversible barrel shifter. In any case, because of multifaceted nature and space issue we appeared here outline for (4,2) reversible barrel shifter. The circuit fills in as takes after: Each phase of Fredkin entryway

moves the contribution as indicated by the control estimation of sk . Assume, to outline a (4, 2) shifter which takes i_0, i_1, i_2, i_3 as information inputs and $s_0s_1 = 11$ as select information. So the information will be moved $2^0+2^1 = 3$ times to one side. In this way the arrangement of the movement/turn operation will be $i_1i_2i_3 i_0$ for the main stage and after that $i_3i_0i_1i_2$ for the following. Then again, for the select information $s_0s_1 = 00$, the info grouping will stay same for both phases of multiplexing. Consequently, each Fredkin door picks between two information lines it gets and plays out the suitable operation as indicated by the select contribution of that specific stage. Henceforth, for the primary (Stage 0) of above (4:2) shifter, the main Fredkin entryway will either choose information i_0 or i_1 , the second one will do either i_1 or i_2 et cetera. Every single other stage play out the choice assignment similarly.

Conversion unit

We have composed a reversible change unit that serves at the same time as a sign size to-two's supplement unit and a two's supplement to-sign greatness unit. Of note is that our unit plays out a reversible mapping, f , with the accompanying altered point:

$(10...0)=10...0$ This implies, for an n bit signed integer:

$$f([-2n-1]2's\ complement) = [-0]sign-magnitude\ f$$

$$([-0]sign-magnitude) = [-2n-1]2's\ complement$$

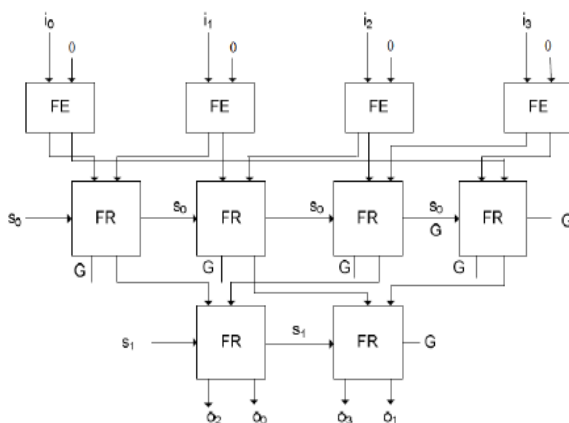


Fig2-Proposed Design of reversible barrel shifter[9]

Our configuration requires two of the 28 bit reversible converters (one for every trailing critical), and a solitary 29 bit converter for the yield of the 28 bit full snake. Before the following reversible standardization step, this 29 bit sign stretched out whole is changed over back to sign size with a solitary occasion of a 29 bit reversible transformation unit.

28-Bit Ripple Carry Full Adder:

For this usage, we will utilize the Peres door as it is the entryway with the lower quantum cost. The Peres door execution of Full Adder with its comparing quantum expense can be seen underneath:



Fig3-Ripple carry full adder[10]

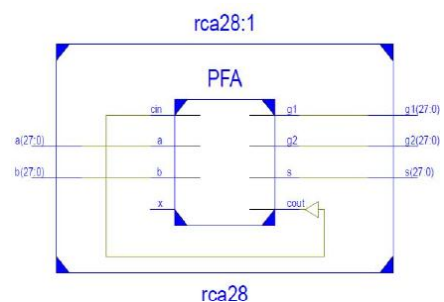


Fig-4 Schematic view of PFA

Reversible Normalization

After the entirety of the trailing huge has been changed over once more into sign-extent representation, the sign piece is associated specifically to the last stage as the indication of the drifting point total, and the greatness may should be standardized. This standardization step may include either left moving or right moving. On the off chance that a right move is required, just a right move of a solitary position will be required. Generally a left move of potentially a few put might be required. Synchronous drifting point snake engineering may finish this conduct utilizing synchronous driving one indicators and synchronous movement registers, however with regards to our

offbeat reversible configuration strategy; we outline a totally no concurrent reversible standardization unit.

Reversible Rounding

Our reversible adjusting unit plays out the reversible round toward zero adjusting calculation indicated in the IEEE754standard. This unit is a pseudo unit, in that it comprises of no additional equipment: It works essentially by changing a portion of the info bits into junk yields by disregarding them by and large.

IV.EFFICIENT APPROACHES TOWARDS EFFICIENT FLOATING POINT MULTIPLICATION UNIT AND DIVISION UNIT

Reversible Multiplication Unit-

For to plan single accuracy drifting point multiplier, there is prerequisite of productive 24x24 piece number multiplier. Operand deterioration methodology is productive for the propose reversible outline of 32 bit drifting point multiplier. To outline the reversible 24x24 (AxB) bit multiplier, the qualities are partitioned into three subgroups of 8 bits each. Subsequently, the 24x24 piece reversible increase can be performed through nine reversible 8x8 piece Wallace tree multipliers, of which yields are then summed. There are three reasonable stages in Wallace tree duplication: incomplete item pressure utilizing 4:2 compressors, Partial item era, full & half adders and afterward the last expansion stage to create the item. In this work there is necessity of advancement at each of these three phases.

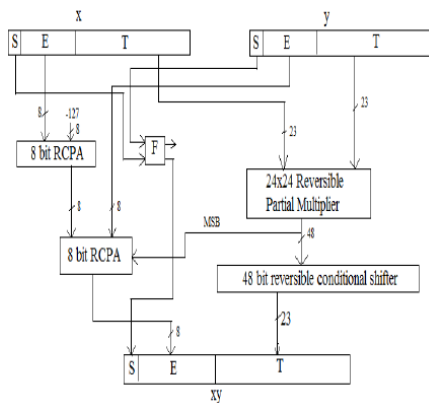


Fig-5 Algorithm for floating point multiplication

Reversible Division Unit(Conventional)

Let,

Dividend, $A = A_0:A_1A_2:::A_n$

Divisor, $D = D_0:D_1D_2:::D_n$

Remainder, $R = R_0:R_1R_2:::R_n$

Quotient, $Q = Q_0:Q_1Q_2:::Q_n$

The operands are assumed to be positive, normalized fractioned fractions.

So, $A_0 = D_0 = 0$ and $A_1 = D_1 = 1$. The quotient is Positive and the partial remainder R is a signed fraction, and R_0 is the sign bit with R being represented in 2's complement form.

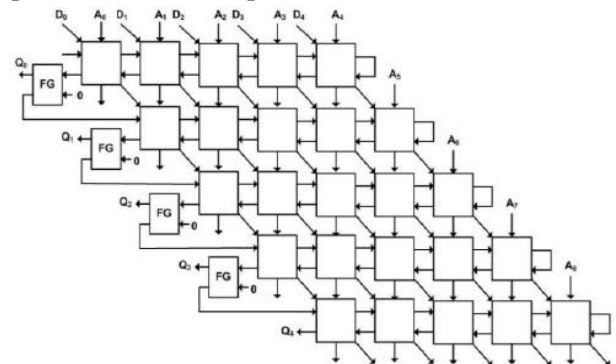


Fig-6 Conventional Division Array :8-bit Dividend and 4-bit Divisor[11]

Proposed reversible divider using high speed division array

The reversible divider utilizing rapid division exhibit is planned by some significant changes of the configuration past area. The convey swell time, which is relative to n, has been overlooked in this configuration. The fractional leftover portion R is not created in every column of the exhibit, but rather is spoken to by two twofold vectors S and C which, if included, would deliver the right incomplete leftover portion at that line level. A solitary convey look ahead circuit is utilized to decide from the S and C vectors what the convey sign would encourage, the determination of the indication of the subsequent fractional leftover portion, the remainder bit for that line level, and the control (include or subtract divisor) to the following line. Subtraction of the divisor is executed utilizing

2's supplement expansion as a part of the customary cluster. Three sorts of cell, specifically, A phone, S cell and CLA cell have been utilized as a part of the fast exhibit plan. The Ajs (profit) are contribution from the top, and the supplemented Djs (divisor) are contribution through the inclining lines. Addition or subtraction is to be performed in the A cells

Results and Statistics

We practically checked every unit furthermore calculation. For increase and division unit we gave proposed calculation. Xilinx 13.2 is utilized for recreation reason. Additionally the investigation is done as far as quantum cost, waste yields, consistent inputs, and speed and defers parameter. For drifting point counts IEEE 754 standard is utilized.

Reversible addition algorithm-

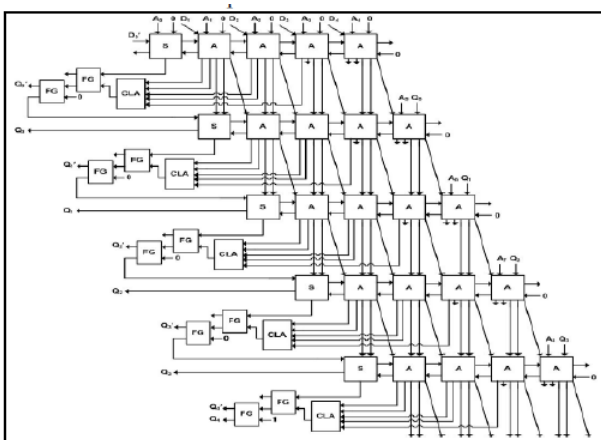


Fig-7 Reversible High Speed Division Array[11]

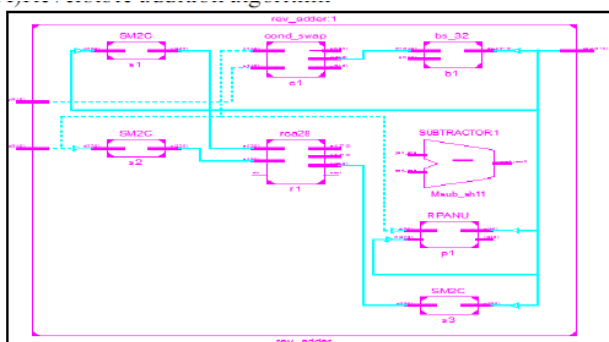


Fig-8)RTL Schematics of addition algorithm

Table III-Cost Measurements For The Reversible modules

Components	Quantum Cost	Constant Inputs	Garbage Outputs
Signed Conversion Unit	140	28	28
28 bit adder	164	52	52

Table IV- Analysis Of Different modules

Designs	Delay	Levels Of Logic
Existing Irreversible Design 28 bit RCA	45.474ns	30
Proposed Reversible Design 28 bit RCA	29.009ns	19
Reversible Barrel shifter design	16.684ns	9
Conditional Swap Unit	46.464ns	33
Signed Conversion Units	9.033ns	3
Reversible Normalization Unit	22.583ns	12
Total addition algorithm	46.544ns	33

CONCLUSION

This paper introduces the skimming direct unit agreeing toward IEEE 754 Standard. The sum total of what modules has been outlined in reversible approach to diminish power utilization. Examination of the sum total of what units has been as far as quantum cost, refuse yields, consistent inputs, and speed and defer parameter. The reproduction consequences of expansion unit are given in this paper.

In future the investigation of augmentation unit will be conceivable.

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