

A Novel Implementation of Floating Point Arithmetic Unit by Using Reversible Logic Gates

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Abstract:

The study of reversible circuits holds great promise for emerging technologies. Reversible circuits offer the possibility for great reductions in power consumption, and quantum computers will require logically reversible digital circuits. Many different reversible implementations of logical and arithmetic units have been proposed in the literature, but very few reversible floating-point designs exist. Floating-point operations are needed very frequently in nearly all computing disciplines, and studies have shown floating-point addition to be the most oft used floating-point operation. In this paper we present for the first time a reversible floating-point adder that closely follows the IEEE754 specification for binary floating-point arithmetic. Our design requires reversible designs of a controlled swap unit, a subtracter, an alignment unit, signed integer representation conversion units, an integer adder, a normalization unit, and a rounding unit. We analyze these major components in terms of quantum cost, garbage outputs, and constant inputs.

Keyword:

IEEE754, Reversible logic, Garbage output, Quantum cost, Floating Point, Arithmetic Unit etc.

1.INTRODUCTION:

In past decades, there were several of difficulties and issues occurred in the development of conventional computing technologies. The main difficulty of the conventional computing technologies is power dissipation and it a significant problem in today's computer chip [1]. The advancement in VLSI designs especially in portable device technologies lead to faster, smaller and more complex electronic system design.

In VLSI design, the conventional logic circuits dissipate more power. Reversible logic is a promising computing design paradigm which presents a method for constructing computers that produce no heat dissipation. Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine. The basic principle of reversible computing is that a bijective device with an identical number of input and output lines will produce a computing environment where the electrostatics of the system allow for prediction of all future states based on known past states, and the system reaches every possible state, resulting in no heat dissipation. Reversible computing differs from conventional computing in that it performs the computation in a logically reversible way: The output of a (fully) reversible circuit always uniquely identifies the input. Circuits can take advantage of this logical reversibility to reduce power by reusing the information instead of discarding it:

Landauer showed that any time a bit of information is discarded, it equates to some quantum of energy lost as heat [1]. Moreover in 1973, Bennett has shown that this energy loss can be reduced or even removed if the circuits are designed using reversible gates [2]. An arithmetic circuit which performs digital arithmetic operations has many applications in digital coprocessors, application specific circuits, etc. Because of the advancements in the VLSI technology, many complex algorithms that appeared impractical to put into practice have become easily realizable today with desired performance parameters so that new designs can be incorporated. Modern computers use conventions for representing non integer numbers, the most widespread of which is the IEEE 754 Standard for Floating-Point calculations.

This standard defines binary representation for floating-point numbers of varying precision, giving specific examples of the binary32 (or single precision) format, binary64 (or double precision) format, and it defines operations on floating-point numbers. The essential components in IEEE 754 standard floating point numbers are the sign, the exponent, and the mantissa.

Table I-Bit Range For Floating-Point Values

	Sign	Exponent	Fraction	Bias
Single precision	1(31)	8(30-23)	23(22-00)	127
Double precision	1(63)	11(62-52)	52(51-00)	1023

Table II-Floating Point Number Representation

32 Bit		
Sign	Exponent	Mantissa
1 bit	8 bit	23 bit

There are four types of exceptions that arise during floating point operations. Whenever the result cannot be shown as a definite number in the precision format of the destination the Overflow exception is occurred. The Underflow exception take place when an intermediate result is very small to be calculated correctly. When zero divides a finite nonzero number, the Division by zero exception arises. The Invalid operation exception is raised if the given inputs are not appropriate for the operation to be performed. The remaining paper is structured as follows. Section II consist of important details of reversible logic design, with coverage of some reversible logic primitive gates. Section III provides details of floating-point addition algorithm and architecture. Section IV outlines approaches towards multiplier and divider design. Section v presents our final measurements, a brief analysis of the architecture, and direction for future work. Section VI concludes the paper with our list of references.

II. BACKGROUND WORK

Many traditional logic gates such as the AND, OR, NAND, NOR, and XOR gates are fundamentally irreversible.

That is to say that the output combination of any of these gates does not expose the input combination that caused the output. Thus we have a need for primitive reversible logic gates.

A.Reversible Gate:

Reversible gates are the circuits having one to-one relationship between vectors of input and output. Therefore from output vector state we can reconstruct the vector of input states.

B. Quantum Cost:

Every quantum circuit is built using 1X1 and 2X2 quantum primitives and its cost is calculated as a total sum of 2X2 gates used since 1X1 gate has no cost, i.e., zero. Basically the quantum primitives are matrix operation which is applied on qubits state. All the gates of the form 2X2 has equal quantum cost and the cost is unity, i.e., one [3]. Since every reversible gate consists of 1X1 or 2X2 quantum gate, the quantum cost of a reversible design calculates the total number of 2X2 gates used. The quantum costs of Feynman gate [4], Peres gate [5] and DPG gate (as full adder) [6] are one, four and six respectively.

C. Garbage Output:

Unwanted or unused output of a reversible gate (or circuit) is known as garbage output, i.e., the output(s) which is(are) needed only to maintain the reversibility is(are) known as garbage output(s).

D. Delay:

The maximum number of gates in a route from any input signal line to any output line is known as delay of a circuit. At the beginning, each gate performs the design computation in one unit time. Secondly, all inputs to the circuit are known before the computation begins.

E. Popular Reversible Gate:

1) Feynman Gate:

The input and output vectors of 2x2 Feynman Gate (FG) [4] are $(I_p)_v$ and $(O_p)_v$ respectively and can be defined as follows:

$(Ip)v = \{a\}$ and

$(Op)v = \{a \text{ xor } b\}$

2)Peres Gate:

The input and output vectors of 3x3 Peres Gate (PG) [5] are $(Ip)v$ and Ov respectively and can be defined as follows:

$(Ip)v = \{a,b,c\}$ and

$(Op)v = \{a, a \text{ xor } b, a \text{ xor } c\}$

The 3 bit Peres gate has Quantum cost of 4.

3)Double Peres Gate

Input vector, $(Ip)v$ and output vector, $(Op)v$ of 4x4 Double Peres Gate (DPG) [6] are defined as follows:

$(Ip)v = \{a,b,c,d\}$ and

$(Op)v = \{a, a \text{ xor } b, a \text{ xor } c, (a \text{ xor } b) \text{ xor } a \text{ xor } c\}$

4) Fredkin Gate

Input vector, $(Ip)v$ and output vector, $(Op)v$ of 3x3 Fredkin Gate (FR) are defined as follows:

$(Ip)v = \{a,b,c\}$ and

$(Op)v = \{a, a' \text{ xor } b, a' \text{ xor } c\}$

5)HNG Gate

Input vector, $(Ip)v$ and output vector, $(Op)v$ of 4x4 HNG are defined as follows:

$(Ip)v = \{a,b,c,d\}$ and

$(Op)v = \{a, b \text{ xor } c, (a \text{ xor } b) \text{ xor } a \text{ xor } d\}$

III.FLOATING POINT ADDITION:

Given two floating-point numbers to be added, the IEEE754 Standard for Floating-Point Arithmetic details how their sum can be found [7]. First, if the exponents are not equal, the smaller is incremented until it aligns with the larger. To align the floating-point number with the smaller exponent without altering its value, its respective trailing significand must be shifted one place to the right for every time the exponent is incremented. Once the exponents are equal, the significands can be summed. The sum is then normalized and rounded. Fig. 1 illustrates the block-level schematic of the architecture our proposed reversible floating-point adder design uses

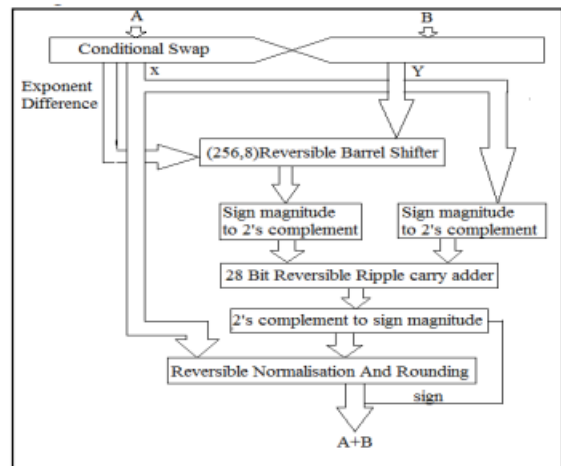


Fig-1 Proposed design of reversible addition architecture

A) Reversible Conditional Swapping:

The first step in our reversible floating-point adder architecture is to swap the floating-point operands conditionally and reversibly. The rest of the architecture operates assuming that X is the floating-point number with the greater exponent, and Y is the floating-point number that possibly needs to be aligned with X. The exponents of the two floating-point numbers both are unpacked and expanded to nine bits. In order to find their difference the 812 exponent that is the minuend is complemented using two's complement, and with it the difference is calculated. The nine HNG gates implement the reversible subtracter circuit [8]. The sign bit of the difference of the exponents acts as the condition (control) by which the two entire floatingpoint numbers are swapped: If $expA < expB$, then the floating point numbers will swap position, otherwise $expA \geq expB$ and the floating-point numbers are passed through to the next stage without swapping.

B) Reversible Barrel Shifter:

In our proposed system we require (256,8) reversible barrel shifter. But due to complexity & space problem we shown here design for (4,2) reversible barrel shifter. The circuit works as follows: Each stage of Fredkin gate shifts the input according to the control value of s_k . Suppose, to design a (4, 2) shifter which takes i_0, i_1, i_2, i_3 as data inputs and $s_0 s_1 = 11$ as select

input. So the input will be shifted $2^0 + 2^1 = 3$ times to the left. Thus the sequence of the shift/rotate operation will be $i_1i_2i_3 i_0$ for the first stage and then $i_3i_0i_1i_2$ for the next. On the other hand, for the select input $s_0s_1 = 00$, the input sequence will remain same for both stages of multiplexing. Thus, each Fredkin gate chooses between two input lines it receives and performs the appropriate operation according to the select input of that particular stage. Hence, for the first stage (Stage 0) of above (4:2) shifter, the first Fredkin gate will either select input i_0 or i_1 , the second one will do either i_1 or i_2 and so on. All other stages perform the selection task in the same way.

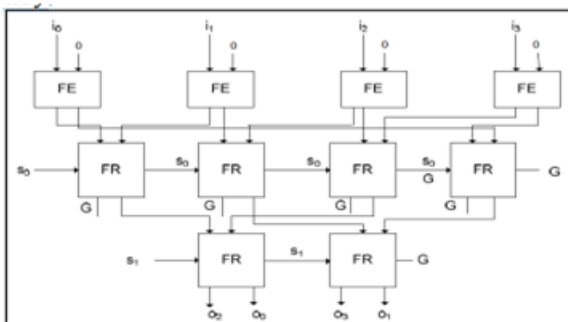


Fig2-Proposed Design of reversible barrel shifter[9]
C) Conversion unit

We have designed a reversible conversion unit that serves simultaneously as a sign magnitude-to-two's complement unit and a two's complement-to-sign magnitude unit. Of note is that our unit performs a reversible mapping, f , with the following fixed point: $f(10...0) = 10...0$. This implies, for an n bit signed integer:

$$f([-2n-1]2^{\prime} \text{ s complement}) = [-0] \text{ sign-magnitude}$$

$$f([-0] \text{ sign-magnitude}) = [-2n-1]2^{\prime} \text{ s complement}$$

Our design requires two of the 28 bit reversible converters (one for each trailing significant), and a single 29 bit converter for the output of the 28 bit full adder. Before the ensuing reversible normalization step, this 29 bit sign extended sum is converted back to sign magnitude with a single instance of a 29 bit reversible conversion unit.

D.28-Bit Ripple Carry Full Adder

For this implementation, we will be using the Peres gate as it is the gate with the lower quantum cost. The Peres gate implementation of Full Adder with its corresponding quantum cost can be seen below:



Fig3-Ripple carry full adder[10]

E. Reversible Normalization:

After the sum of the trailing significands has been converted back into sign-magnitude representation, the sign bit is connected directly to the final stage as the sign of the floating-point sum, and the magnitude may need to be normalized. This normalization step may involve either left shifting or right shifting. If a right shift is required, only a right shift of a single position will be required. Otherwise a left shift of possibly several places may be required. A synchronous floating-point adder architecture might accomplish this behavior using synchronous leading-one detectors and synchronous shift registers, but in keeping with our asynchronous reversible design methodology, we design a completely asynchronous reversible normalization unit.

F. Reversible Rounding:

Our reversible rounding unit performs the reversible round toward zero rounding algorithm specified in the IEEE754 standard. This unit is a pseudo unit, in that it consists of no extra hardware: It operates simply by transforming some of the input bits into garbage outputs by ignoring them altogether.

IV.EFFICIENT APPROACHES TOWARDS EFFICIENT FLOATING POINT MULTIPLICATION UNIT AND DIVISION UNIT:

A)Reversible Multiplication Unit For to design single precision floating-point multiplier, there is requirement of efficient 24x24 bit integer multiplier. Operand

decomposition approach is efficient for the propose reversible design of 32 bit floating point multiplier. To design the reversible 24x24 (AxB) bit multiplier, the values are divided into three subgroups of 8 bits each. Thus, the 24x24 bit reversible multiplication can be performed through nine reversible 8x8 bit Wallace tree multipliers, of which outputs are then summed.

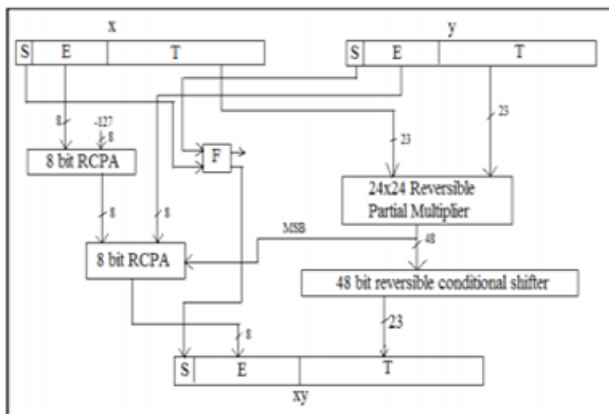


Fig-4 Algorithm for floating point multiplication

There are three conceptual stages in wallance tree multiplication: partial product compression using 4:2 compressors, Partial product generation, full & half adders and then the final addition stage to generate the product. In this work there is requirement of optimization at each of these three stages.

B) Reversible Division Unit(Conventional)

Let, Dividend, $A = A_0:A_1A_2:::A_n$

Divisor, $D = D_0:D_1D_2:::D_n$

Remainder, $R = R_0:R_1R_2:::R_n$ Quotient,

$Q = Q_0:Q_1Q_2:::Q_n$

The operands are assumed to be positive, normalized fracsigned fractions. So, $A_0 = D_0 = 0$ and $A_1 = D_1 = 1$. The quotient is positive and the partial remainder R is a signed fraction, and R_0 is the sign bit with R being represented in 2's complement form.

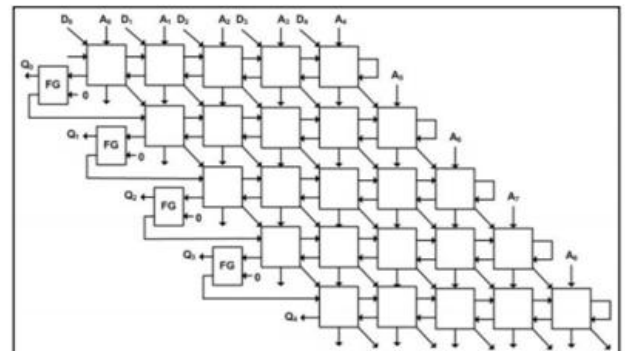


Fig-5 Conventional Division Array :8-bit Dividend and 4- bit Divisor[11]

C) Proposed reversible divider using high speed division array

The reversible divider using high speed division array is designed by some major modifications of the design previous section. The carry ripple time, which is proportional to n, has been omitted in this design. The partial remainder R is not developed in each row of the array, but is represented by two binary vectors S and C which, if added, would produce the correct partial remainder at that row level. A single carry-look ahead circuit is used to determine from the S and C vectors what the carry sign would be, facilitating the determination of the sign of the resulting partial remainder, the quotient bit for that row level, and the control (add or subtract divisor) to the next row. Subtraction of the divisor is implemented using 2's complement addition as in the conventional array. Three types of cell, namely, A cell, S cell and CLA cell have been used in the high speed array design. The A_j s (dividend) are input from the top, and the complemented D_j s (divisor) are input through the diagonal lines. Addition or subtraction is to be performed in the A cells.

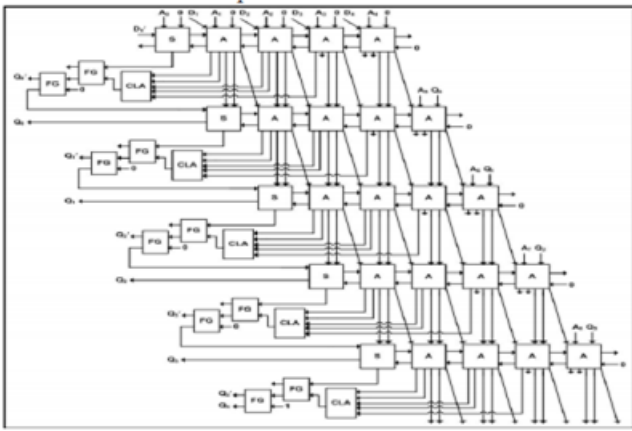


Fig-6 Reversible High Speed Division Array[11]

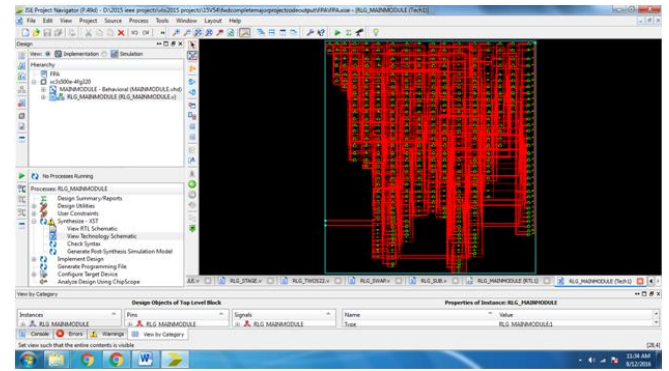


Figure 9: Technology schematic of proposed floating point adder

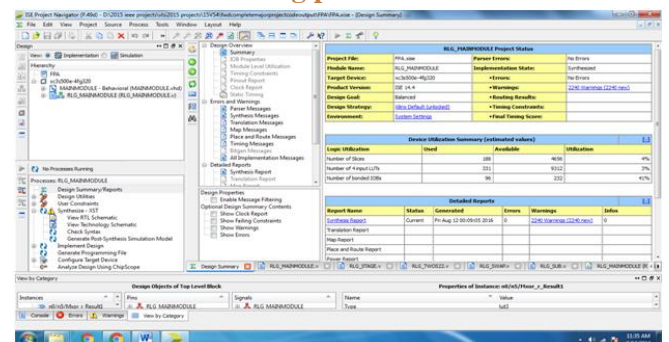


Figure 10: Synthesis report of floating point adder

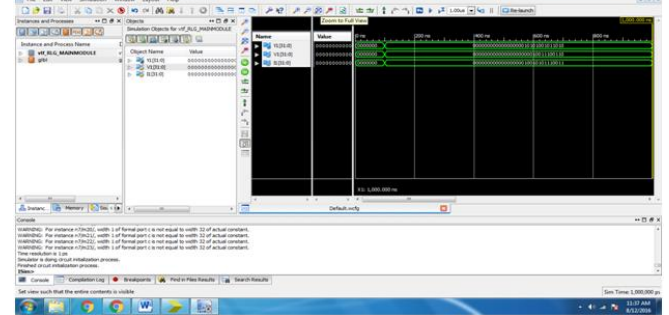


Figure 11: simulated outputs for proposed floating point adder

CONCLUSION:

Floating point arithmetic is one of the most important units in modern day digital systems. Many researchers have proposed various approaches which includes the use of reversible logic in the design of arithmetic unit. This paper presents the floating point unit according to IEEE 754 Standard. All modules has been in reversible way to reduce power consumption. Analysis of all units has been in terms of quantum cost, garbage outputs, constant inputs, speed and delay parameter.

V.SIMULATION RESULTS

The corresponding simulation results of the floating point adders are shown below. All the synthesis and simulation results are performed using Verilog HDL. The synthesis and simulation are performed on Xilinx ISE 14.4. The simulation results are shown below figures.

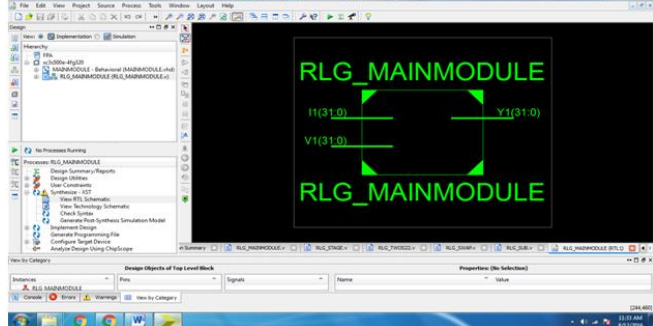


Figure-7: RTL schematic of Top-level of proposed floating point adder

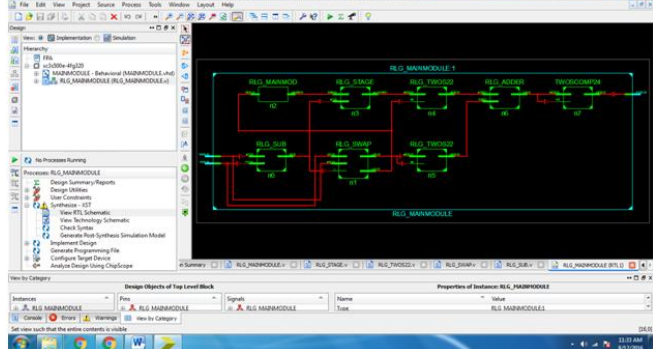


Figure 8: RTL schematic of Internal block of proposed floating point adder

The simulation results of addition unit is provided in this paper. Most of the designs using the reversible logic architecture optimize the delay, latency and the area utilization. In future the analysis of multiplication unit will be possible.

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