ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Efficient Design and Implementation of Modified Novel Bit Adder in QCA

Maddela Prem Kumar
M.Tech Student
Dr. K.V. Subba Reddy Institute of Technology.

A .N. Naga Jyothi, M.Tech,
Assistant Professor
Dr. K.V. Subba Reddy Institute of Technology.

Abstract:
Moore's law expresses that the quantity of transistors that could be incorporated into a solitary pass on would become exponentially with time. Subsequently this causes expanding computational many-sided quality of the chip and physical impediments of gadgets, for example, power utilization, interconnect will turn out to be extremely troublesome. As indicated by late examination as far as possible for transistor size might be come to.

In this way, it may not be conceivable to proceed with the guideline of Moore's law and multiplying the clock rate for at regular intervals. So with a specific end goal to defeat this physical cutoff of CMOS-VLSI outline an option methodology is Quantum speck Cellular Automata (QCA). In ALU snake assumes an essential part. In this study a double viper is taken for investigation and another snake is outlined based upon QCA innovation. This changed novel piece viper is actualized into ALU structure. The point of this proposed procedure is that to diminishing number of dominant part doors utilized as a part of the outline.

This will prompt lessen number of QCA cells so that aggregate region of ALU circuit can be minimized contrast with past outlines. It additionally accomplishes diminished force utilization and rapid exhibitions than all other existing ALU outline which utilizes ordinary full adder.

Index Terms-Moore's law, CMOS, Area, power consumption, Quantum dot Cellular Automata (QCA), Full adder, ALU.

INTRODUCTION

A. CMOS Technology

Microprocessor fabricating procedures was administered by Moore's law, and thus microchip execution till now. Today numerous coordinated circuits are produced at 0.25-0.33 micron forms. Yet, late studies demonstrate that as ahead of schedule as 2010, the physical furthest reaches of transistor measuring might be come to [2]. However the execution of different circuits in current CMOS-based architectures is near achieving the farthest point. On the off chance that the element size of transistors is further lessened to a nanometer, it will create quantum impacts, for example, burrowing. Further, amid gadget scaling process because of the impacts of wire resistance and capacitance, the interconnections never scale consequently.

Expansion is a fundamental operation numerous Digital, Analog, or Control framework [9]-[12]. Quick and exact operation of all advanced framework relies on upon the execution of adders .The primary capacity of viper is to accelerate the expansion of fractional items created amid increase operation. Consequently enhancing the pace by decrease in region is the principle territory of exploration in VLSI framework plan.

B. An Introduction to QCA Technology

As another option to CMOS-VLSI, a methodology called the quantum cell automata (QCA) is created in 1993[1] to processing with quantum dabs. Not at all like routine PCs in which data is exchanged starting with one place then onto the next by electrical current, QCA exchanges data by method for proliferating a polarization state starting with one cell then onto the

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

next cell [7].The charge dissemination in every cell is adjusted along one of two opposite tomahawks, so that the paired data can be encoded by utilizing the condition of the cell.

Tree snake is a substitute to ordinary adder, because by utilizing tree structure conveys are created in parallel and quick calculation is acquired to the detriment of expanded range so control utilization is additionally expanded. The fundamental preferred standpoint of this outline is that the convey tree lessens the quantity of rationale levels (N) by creating the conveys in parallel. The parallel- prefix tree adders are more good as far as rate because of the intricacy O (log2N) delay through the convey way contrasted with that of different adders [6].

C. 1 Bit ALU Architecture

The Arithmetic Logic Unit (ALU) plays out the essential number-crunching and intelligent operation. The ALU comprises of number-crunching extender, coherent extender and a full viper which is appeared in Fig. l. Three control signs will choose the operation of the ALU. M is the mode control variable which select amongst number juggling and sensible operations. Sl as are choice line utilized as a part of blend with M to choose between the eight number juggling and coherent operation the ALU supports. Detail about Arithmetic and Logical Extender is clarified in [8].

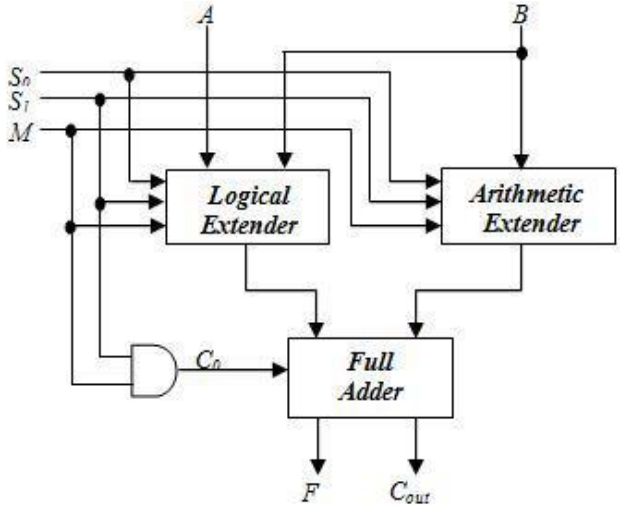

Fig 1: Architecture of ALU

BACKGROUND

A. Basics of QCA

The fundamental component of QCA strategy is QCA cell. In QCA cell every cell is having four quantum specks [3] and in which two are free electrons. Fig.2 demonstrates the QCA cell outline. A quantum-dab cell automata (QCA) cell is a square nanostructure of electron wells. The four spots are situated in the four corners of this square structure.

The cell can be charged by utilizing free electrons, since outer force supply is not gave here. The electrons passage to legitimate area by utilizing the timing instrument amid the clock move. In this way there exist two electrons in the QCA cell as appeared in Fig. 2 and area of the electrons in the QCA cell is to speak to the twofold states. These two courses of action are speaking to rationale I and rationale 0 separately by utilizing which the double data can be encoded.

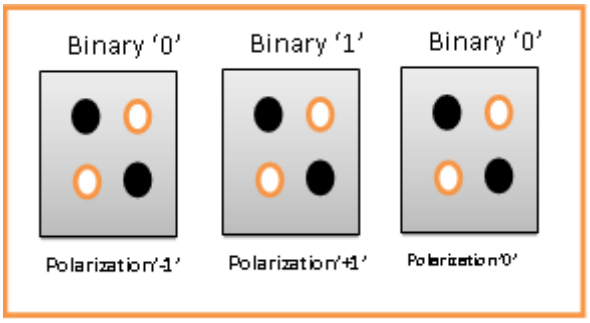

Fig 2: QCA Cell Polarization

Larger part entryway and Inverter are the general rationale components in QCA by utilizing which we can determine any rationale circuits utilizing coupled quantum dab cell. Inverter is spoken to in Fig. 3 and Majority entryway is in Fig. 4.

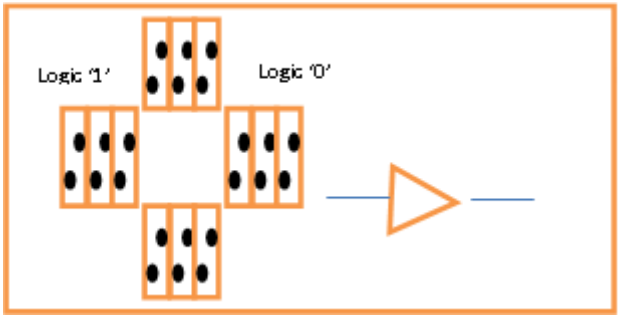

Fig 3: inverter

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

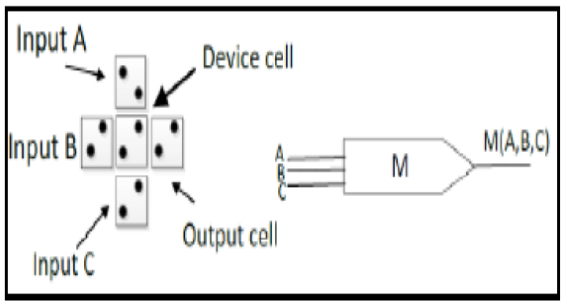

Fig 4: majority gate

In QCA outline two sorts of hybrid is conceivable, for example, named coplanar hybrid and multilayer hybrid separately.

EXISTING QCA ADDERS

A few outlines of adders in QCA are existing. The RCA [9], [11] and the CFA [10] process n-bit operands by falling of n full-adders (FAs). A CLA design framed by 4-bit cuts was introduced [9].n-bit CLA has a computational way made out of 7 + 4 x (log4 n) fell MGs and one inverter The parallel-prefix BKA [11] misuses more effective fundamental CLA rationale structures. Its principle advantage over the beforehand depicted adders; the BKA can accomplish lower computational postponement. At the point when n-bit operands are prepared, its most pessimistic scenario computational way comprises of 4 x log2 n - 3 fell MGs and one inverter.

With the primary target tradeoff amongst region and postponement, the mixture snake (HYBA) depicted in [12] joins a parallel- prefix viper with the RCA. For n-bit operands, this engineering has a most exceedingly awful computational way comprising of 2xlog2 n +2 fell MGs and one inverter. At the point when the technique proposed in [13] was misused, the most pessimistic scenario way of the CLA is diminished to 4 x (Iog4 n) + 2 x (Iog4 n) - 1 MGs and one inverter. This methodology can likewise be connected to plan the BKA. For this situation the general range is decreased regarding [11], yet keeping up the same computational way.

By applying the decay strategy [14], the computational ways of the CLA and the CF An area lessened to 7 + 210g2 (n/8) MGs and one inverter and to (nil) + 3 MGs and one inverter, individually.

As of late created novel n bit viper [5] has separate structure for convey and whole era. This snake has 5n-4 number of MG's and n inverters for n bit adders. One issue in this structure is it won't create right yield for LSB bit mix of info (aObO=Ol).for case for including 2 numbers, for example, 2(10) and 3 (11) the genuine yield is 5(101) however this snake [5] will deliver entirety as 4(100).

PROPOSED QCA ADDER

In this segment, we propose a two new QCA expansion calculation and the comparing good for nothing QCA viper structure that lessens the quantity of the greater part entryways and inverters required for existing plans [5] and wipe out previously mentioned disadvantage moreover.

A. Modified Novel Bitadder 1

To present proposed Modified novel piece viper 1 - n bit engineering first it is composed a 2 bit fundamental module taking into account proposed calculation. give us a chance to consider 2 operands, for example, A=a1aO and B=b1bO and we outlined proposed 2bit module as appeared in fig 5(a).For every piece the convey is created by utilizing one dominant part door. Total is figured by falling of 3 MG's.

Given three inputs a, b, and c, the MG plays out the rationale capacity reported in (1) gave that all information cells are related to the same clock signal c1kx (with x extending from 0 to 3)

$$M(a,b,c)=a.b+b.c+c.a \quad (1)$$

To make a n-bit viper, let consider two n- bit addends A = an-I, ... , aO and B = bn-I, ... , bOand for i = n - 1, ... , 0 and we mastermind n proposed one-piece adders vertically in a section which is appeared in fig5(b) and (c)respectively.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

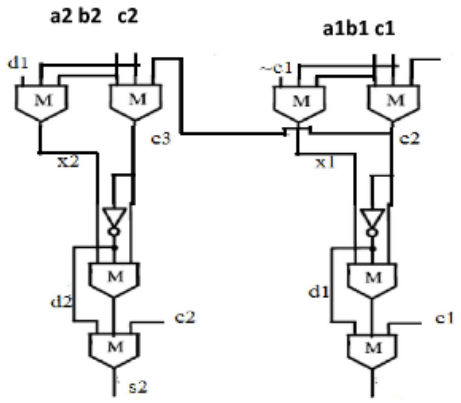

Fig 5(a): Modified novel bit adder 1: 2 bit basic module

This proposed design can be actualized by utilizing condition (2) and (3)

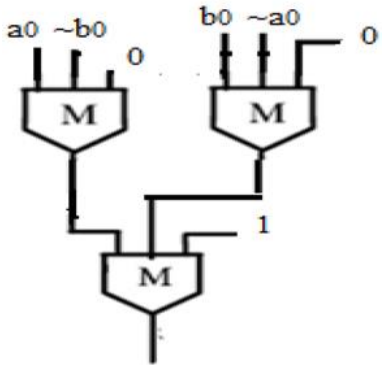

Fig 5(b): Modified novel bit adder 1-Calculation of xO

$C_{i+1}=M(a_i,b_i,c_i)$ (2)

$S_i=M(M(a_i, b_i, c_i \text{ xo } _i, b_i, c_i), d_i), d_i, C_i)$(3)

Where $d_i=\tilde{}\ c_{i+1}$

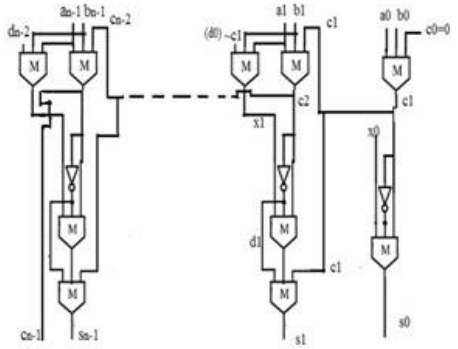

Fig 5(c): Modified novel bit adder I: n bit basic module.

The proposed n bit QCA adder consists of 4n+1 number of majority gates and n+2 inverters. It results in reduced hardware compared to the existing structure and retains the simple clocking scheme.

Modified Novel Bit Adder 2

Here we now present another Modified novel piece viper 2-n bit snake engineering which lessens equipment intricacy contrasted with existing[5] and Modified novel piece snake 1 structure. The essential 2bit module for Modified novel piece snake 2 is appeared in fig 6(a). Here the convey is computed in same route as in proposed 1 structure and whole square is altered which requires two greater part entryways as it were.

This proposed engineering can be actualized by utilizing condition (4) and (5)

$C_{i+1}=M(a_i, b_i, c_i)$ (4)

$S_i=M(M(M(a_i, b_i, d_i),d_i, c_{i-1}), d_i$ (5)

Where $d_i=\tilde{}\ c_{i+1}$

To make a n-bit snake, let consider two n- bit addends A = an-I, ... , aO and B = bn-I, ..., bO and for i = n - 1, ... , 0 and we orchestrate n proposed one-piece adders vertically in a section which is appeared in fig 6(b).

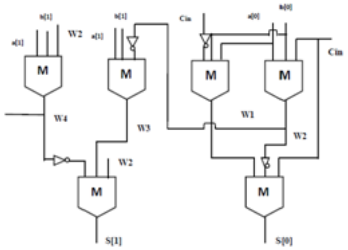

Fig 6(a): Modified novel bitadder 2: 2bit basic module.

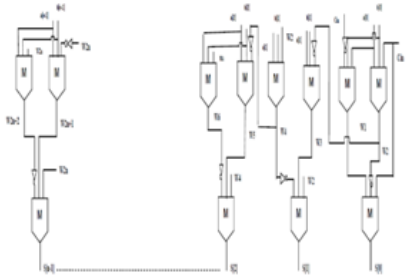

Fig 6(b): Modified novel bit adder 2: n bit adder

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

The proposed n bit QCA snake comprises of 3n number of larger part entryways and n inverters. It results in decreased equipment contrasted with the current [5] structure and prorating the straightforward timing plan.

SIMULATION AND SYNTHESIS RESULTS

Reproduction IS performed by utilizing modelsim6.4a reenactment instrument and the operation is checked for all the info combinations. Fig 7 demonstrates the downside of existing [5] viper i.e. wrong yield for LSB mixes of 01.

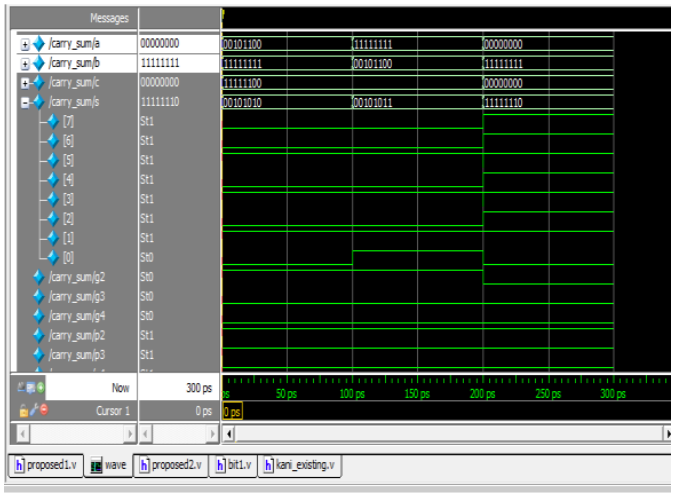

Fig 7: simulation result of existing adder[5]

Modified Novel Bit Adder

Fig 8(a) and 8(b) shows the simulation result of modified novel bit adder 1 and 2 respectively

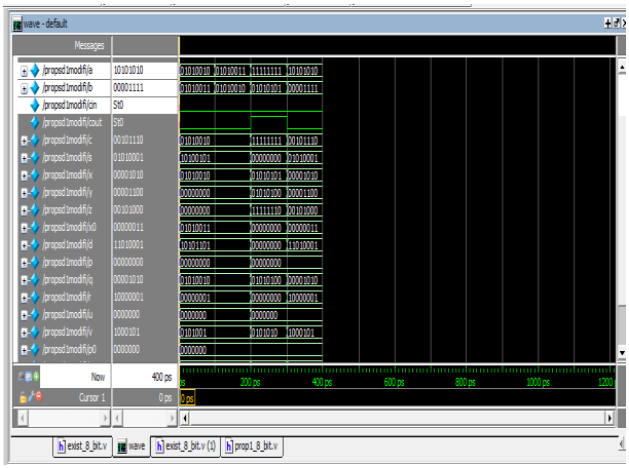

Fig 8(a): simulation result of Modified novel bit adder I

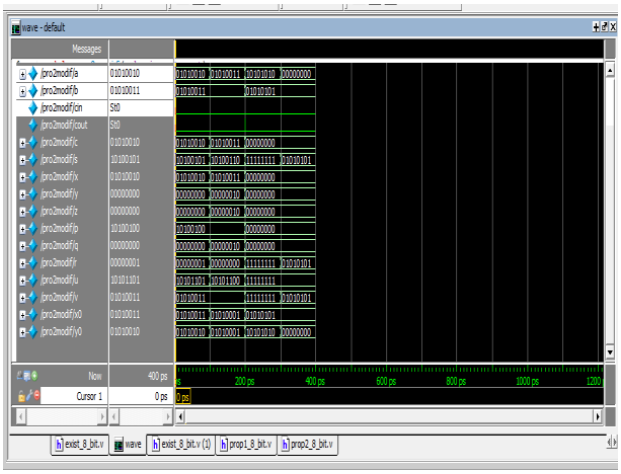

Fig 8(b): simulation result of Modified novel bit adder 2

Amalgamation is performed by utilizing Xilinx ISE 8.1i instrument fig 9(a) and fig 9(b) demonstrates the zone report of Modified novel piece viper 1 and Modified novel piece snake 2 individually. Door include examination is appeared

TABLE 1: COMPARISION FOR GATE COUNTSIN ADDERS

	Existing Adder	Modified Novel Bit Adder 1	Modified Novel Bit Adder 2
Gate Count (Xilinx)(8 bit)	141	102	96

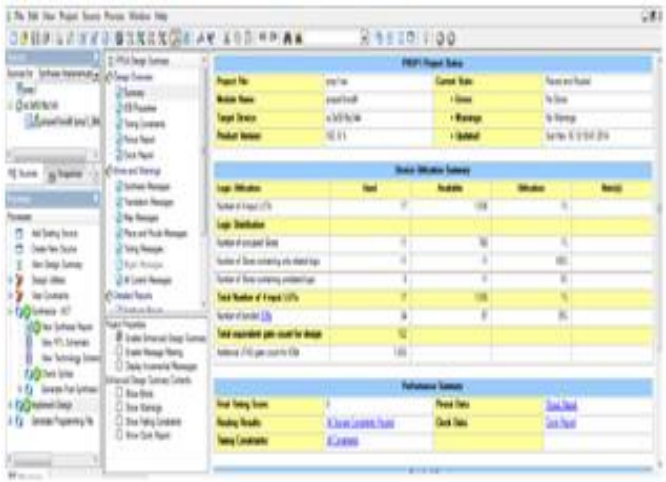

Fig lO(a): Simulation result of proposed ALU

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

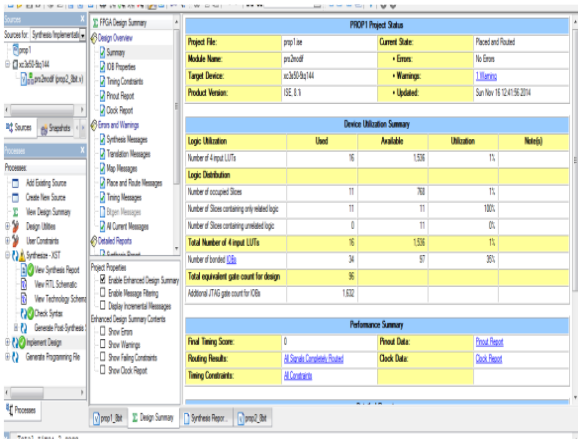

Fig 9(b): Area report of Modified novel bit adder 2

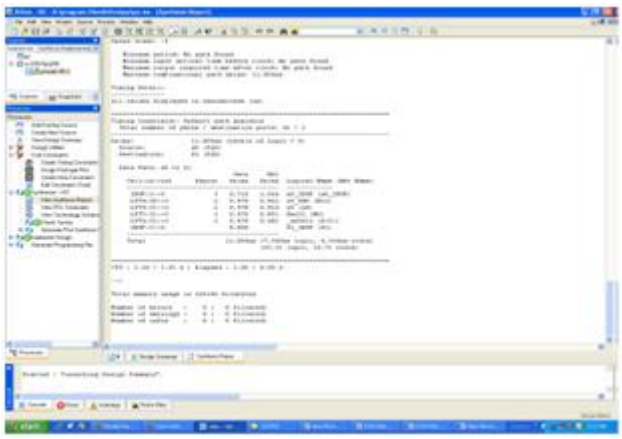

Fig I O(c): Delay report of proposed ALU

ALU Design Using Modified Novel Bit Adder 2

In light of above dialog, changed novel piece viper 2 is the best decision regarding territory and delay. So one piece ALU is composed utilizing Modified novel piece snake 2 .reenactment and region, delay result for proposed ALU is appeared in Fig l0 (a), Fig l0 (b), Fig 1O(c) individually. It accomplishes less region and postponement contrasted with existing ALU [8].

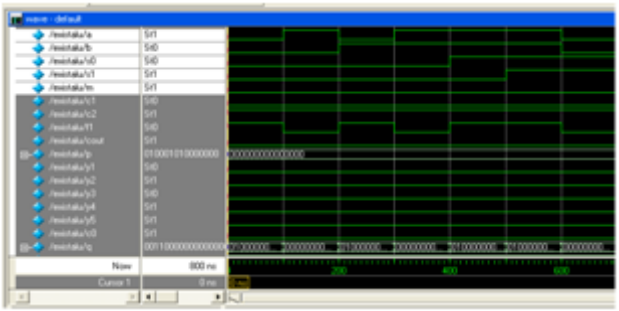

Fig l0 (a): Simulation result of proposed ALU

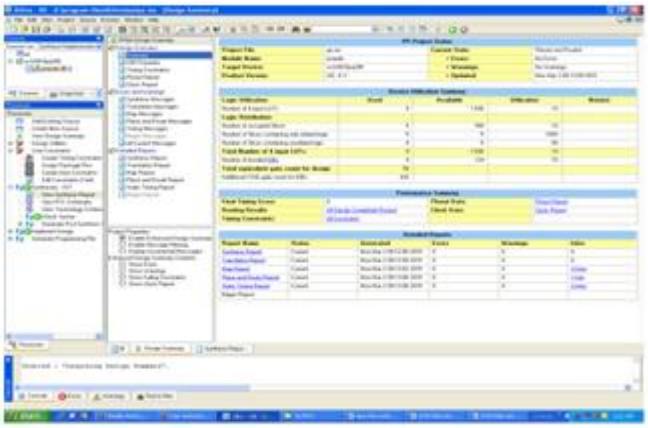

Fig 10 (b): Area report of proposed ALU

CONCLUSION

Another snake in QCA innovation was composed which accomplishes decreased range than all the current QCA adders [5]. The Proposed altered novel piece viper 2 is actualized in I bit ALU circuit to enhance the efficiency. The proposed ALU has all out door tally of 54 which is decreased than existing ALU [8] in which entryway tally is 66.The deferral required for proposed ALU structure is 11.904ns which is not exactly existing in which 15.433ns is needed. The usefulness is checked by utilizing modelsim reenactment apparatus The Future expansion of our work is to outline 4 bit ALU in QCA utilizing Modified novel piece snake 2 structures.

REFERENCE

1. C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernestein, "Quantum cellular automata," Nanotechnology, vol. 4, no. I, pp. 49-57, 1993.

2. The National Technology Roadmap for Semiconductors. Semiconductor Industry Association, 1997.

3. M. T. Niemer and P. M. Kogge, "Problems in designing with QCAs: Layout = Timing," Int. J. Circuit Theory Appl., vol. 29, no. I, pp. 49--62, 2001.

4. K. Walus, G. A. Jullien, and V. S. Dimitrov, "Computer arithmetic structures for quantum

cellular automata," in Proc. Asilomar Conf. Sygnals, Syst. Comput., Nov. 2003, pp. 1435-1439.

5. StefaniaPerri, Pasquale Corsonello, and Giuseppe Cocorullo" Area Delay Efficient Binary Adders in QCA"IEEE transactions on very large scale integration (vlsi) systems, vol. 22, no. 5, may 2014.

6. [6]RajithaChandragiri, 2, P. VenkataLavanya International Journal of Computational Engineering ResearchVol,03Issue, 8 Design and Testing Of Prefix Adder for High Speed Application by Using Verilog HDL.

7. P.D. Tougaw and C.S. Lent. Logical devices implemented using quantum cellular automata. Journal of Applied Physics, 75:1818, 1994.

8. Namit Gupta, K.K. Choudhary and SumantKatiyal "One Bit Arithmetic Logic Unit (ALU) in QCA" Int. J. on Recent Trends in Engineering and Technology, Vol. 8, No. 2, Jan 2013

9. H. Cho and E. E. Swartzlander, "Adder design and analyses for quantum-dot cellular automata," IEEE Trans. Nanotechnol., vol. 6, no. 3,pp. 374-383, May 2007.

10. I-I. Cho and E. E. Swartzlander, "Adder and multiplier design in quantum-dot cellular automata," IEEE Trans. Comput., vol. 58, no. 6, pp. 721-727, Jun. 2009.

11. V. Pudi and K. Sridharan, "Low complexity design of ripple carry and Brent-Kung adders in QCA," IEEE Trans. Nanotechnol., vol. II, no. I, pp. 105-119, Jan. 2012.

12. V. Pudi and K. Sridharan, "Efficient design of a hybrid adder in quantumdot cellular automata," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 9, pp. 1535-1548, Sep. 2011.

13. S. Perri and P. Corsonello, "New methodology for the design of efficient binary addition in QCA," IEEE Trans. Nanotechnol., vol. II, no. 6, pp. 1192-1200, Nov. 2012.

14. V. Pudi and K. Sridharan, "New decomposition theorems on majority logic for low-delay adder designs in quantum dot cellular automata," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 59, no. 10, pp. 678--682, Oct. 2012.