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An Arithmetic and Logic Unit (ALU) Design Using Gate Diffusion Input Technique (GDI)

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ABSTRACT:

This paper presents a design of a 4-bit arithmetic logic unit (ALU) by considering the concept of gate diffusion input (GDI) technique. ALU is the most pivotal and key component of central processing unit and also to the numbers of embedded system and microprocessors. In this, ALU include 4x1 multiplexer, 2x1 multiplexer and full adder designed to implements logic operations, like AND, OR, etc. and also arithmetic operations, like ADD and SUBTRACT,etc. GDI cells are used in the design of multiplexers and full adder and theses are then associated to realize ALU. The simulation is carried out DSCH3.5 and Microwind3.5 simulator using 65nm technologies and compared with previous CMOS logic. The simulation shows that the design is well regulated with less power consumption, less surface area and it is also faster compared to pass transistor and CMOS techniques.

Keywords: ***GDI technique, ALU, Pass transistor gate.***

I. INTRODUCTION:

In the epoch of growing technology and scaling of devices up to nanometre regime, the arithmetic logic circuits have to be designed with compact size, less power and propagation delay. Arithmetic operations are essential and basic functions for any of the high speed low power applications like microprocessors, image processing, digital signal processing, etc. Addition is most important part of the arithmetic unit and approximately all other arithmetic operation includes addition. Thus, the main issue in the design of any arithmetic and logic unit is to have low power, high performance adder cell. There are many Methodologies and topologies proposed to design full adder cell efficiently. This paper makes use of the concept of GDI technique for the design of ALU which uses Multiplexer and Full adder as sub blocks.

II. PREVIOUS WORKS:

There are many types and designs for full adder which are presented at state of the art level and process and circuit level. The Twelve state of the art full adder cells are: conventional CMOS, TG CMOS, CPL, TFA, C2MOS, Hybrid, N-Cell, Bridge, FA24T, DPL and Mod2f.R. Shalem, E. John, and L.K. John, explained conventional CMOS full adder which has 28 transistors. Md. Anwar Hussain, and L.L.K. Singh proposed about Low Power High Speed ALU in 45nm Using GDI Technique and also Its Performance Comparison. We have designed ALU in different way using GDI cells to implement multiplexers and full adder circuit. The input and output sections of this design consist of 4x1 and 2x1 multiplexers and ALU is implemented by using full adder.

III. GATE DIFUSSION INPUT TECHNIQUE

Basic GDI cell is proposed by Morgenshtein as shown in Fig.1 [8]. It is a new method for design of low power digital combinational circuit. This technique is primarily two transistor implementation of complex logic functions which gives in-cell swing restoration under certain operating condition. This approach profits reduction in power consumption, propagation delay and also area of digital circuits is obtained while having low complexity of logic design. The main feature of GDI cell is the source of the PMOS in a GDI cell is not connected to VDD and the source of the NMOS is not connected to GND. Thus GDI cell gives two extra input pins which makes the GDI design more flexible than CMOS design.

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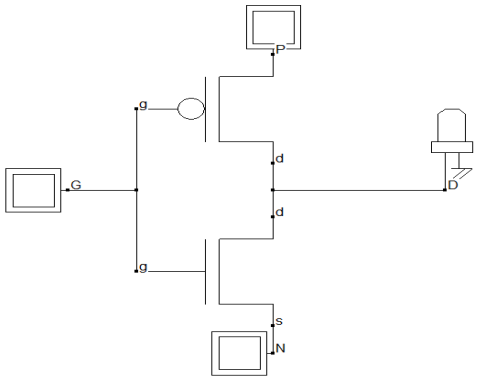

Fig. 1. Basic GDI Cell

GDI cell consists of three inputs - P (input to the source/drain of PMOS), G (common gate input of NMOS and PMOS) and N (input to the source/drain of NMOS). NMOS and PMOS Bulks are connected to N and P respectively. Table 1 shows different logic functions implemented by GDI logic [8] based on different input values. Thus, various logic functions can be implemented with low power and high speed in this GDI technique as compared to conventional CMOS design.

TABLE 1. LOGIC FUNCTIONS OF BASIC GDI CELL

S.No.	N I/P	P I/P	G I/P	Output	Function
1.	0	B	A	A'B	F_1
2.	B	1	A	A'+B	F_2
3.	1	B	A	A+B	OR
4.	B	0	A	AB	AND
5.	C	B	A	A'B+AC	MUX
6.	0	1	A	A'	NOT

Multiplexer:

Multiplexer is a digital switch. It has numbers of input data lines and one output line. The selection of that particular input line is controlled by a set of selection line. There are '2n' input lines and 'n' selection lines whose bit combinations describes which input is selected. Fig 2 shows implementation of GDI cell based 2x1 multiplexer .The 4x1 multiplexer consists of four inputs, two selection lines and one output. Depending on the two selection lines, one output is selected at a time among the four input lines. Fig. 3 shows implementation of 4x1 multiplexer using GDI cell.

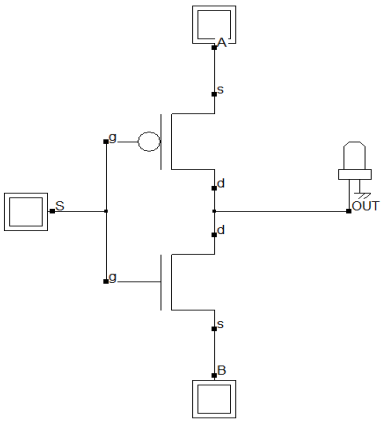

Fig. 2. 2x1 multiplexer using GDI techniques

IV. DESIGN OF ARITHMETIC AND LOGIC UNIT

An arithmetic and logic unit (ALU) is a primary building block of the Central Processing Unit (CPU) of a computer and also the basic microprocessors contains one. It is dependable for performing arithmetic and logic operations such as subtraction, addition, increment, logical OR, decrement, logical AND, logical XOR and logical XNOR. It consists of eight 4x1 multiplexers, four full adders and four 2x1 multiplexers. The design of 4-bit ALU is done in 250nm, n-well CMOS technology. When logic '0'and logic '1' are applied as an input DECREMENT and INCREMENT operations will take place respectively. An INCREMENT operation is analyzed as adding '1' to the addend and DECREMENT is taken as a subtraction operation. For SUBTRACTION Two's complement method is used where complement of B is used. The outputs obtained from the full adder are AND & OR, SUM, EXOR, EXNOR. Fig. 6 shows the block diagram of 4-bit ALU where all the four stages are cascaded with the CARRY bit. Symbolic representation of 4-bit ALU has been shown in fig. 7.The multiplexer stage takes the appropriate inputs depending on the condition of the select signals, and gives it to the full adder which then computes the results.

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TABLE II. OPERATIONS OF ALU

S2	S1	S0	Cin	FUNCTION	OPERATION
0	0	0	0	A+B	ADD
0	0	0	1	A+B+1	ADD WITH CARRY
0	0	1	0	A+B'	SUTRACT WITH BORROW
0	0	1	1	A-B	SUBTRACT
0	1	0	0	A	TRANSFER A
0	1	0	1	A+1	INCREMENT A BY 1
0	1	1	0	A-1	DECREMENT A BY 1
1	0	0	0	A&B	AND
1	0	1	0	A|B	OR
1	1	0	0	A^B	XOR
1	1	1	0	A'	COMPLEMENT

The multiplexer which is at the output stage selects one of the appropriate outputs and direct it to output port. Table II shows the truth table for the operations performed by the ALU considering the status of the select signal. The operation that have been performed and the inputs and outputs being selected are determined by set of three select signals included in the design. Fig 8. Shows multiplexer logic at input port and Fig 9. Shows multiplexer logic at output port. The multiplexer stage selects the suitable inputs based on the condition of the select signals, and gives that input to the full adder which then computes the results. The multiplexer present at the output stage selects the suitable output and route it to output port. Table 2 shows the truth table for the operations performed by the ALU based on the status of the select signal.

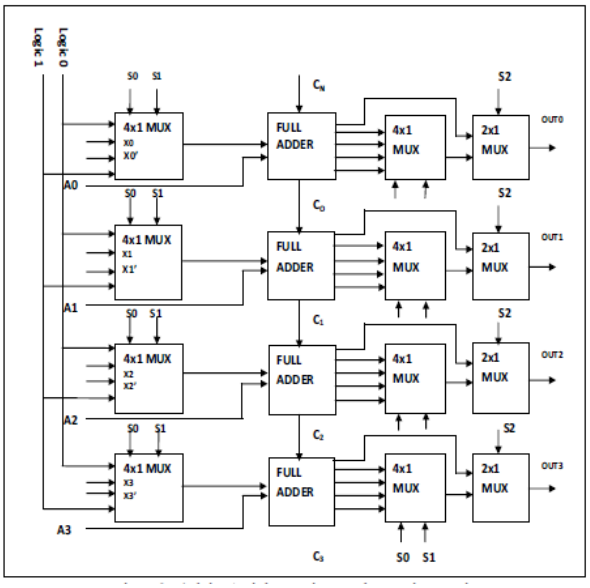

Fig. 6. 4-bit Arithmetic and Logic Unit

The schematic of ALU is designed using schematic editor of DSCH3.5 and Microwind 3.5. It shows connectivity between the components and describes aspect ratios of the transistor that can be customized along with the design. Figure 10 represents the whole schematic view of ALU. The 4-bit ALU consists of two 4-bit inputs, one carry input, three selecting lines, one carry output and four output bits.

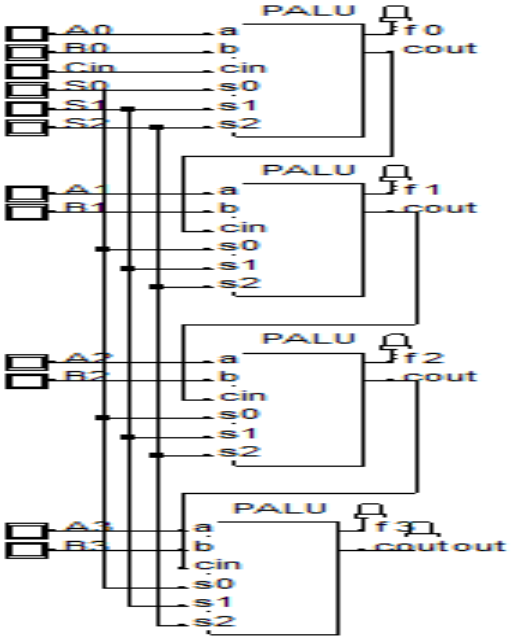

Fig 7. Schematic of 4-bit ALU

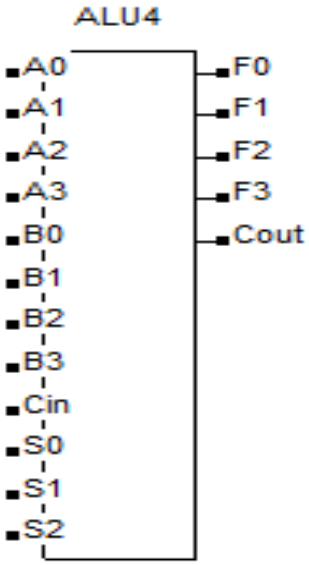

Fig .8. Symbol of 4-bit ALU

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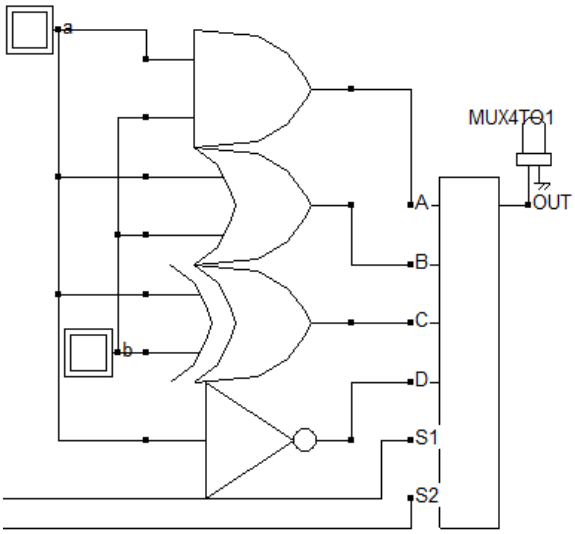

Fig .9. Block diagram of multiplexer logic at the output stage

This paper presents a new approach for design an arithmetic and logic unit using concept of Gate Diffusion Input Technique. Multiplexer is the most relevant device in ALU, for proper selection of input to perform particular operation and for obtaining output accordingly. In previous designs of ALU, the multiplexer unit is either implemented by conventional CMOS logic or by pass transistor logic which confirmed to have high power consumption. This approach gives better result than earlier designs in terms of propagation delay, power consumption as well as area.

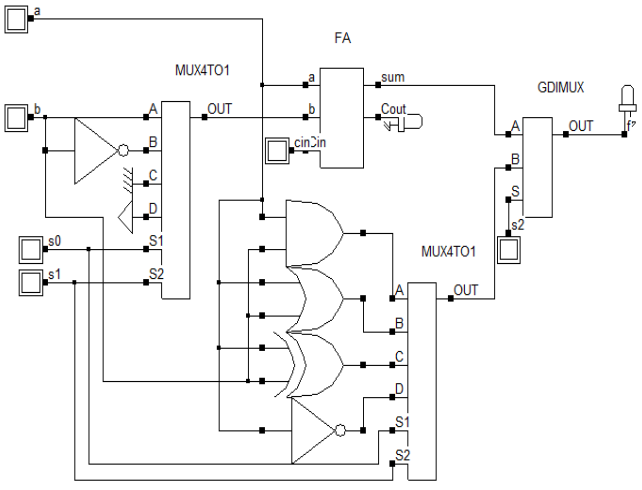

Figure 10. Schematic of 1-bit ALU

V. SIMULATONS RESULTS AND ANALYSIS

This section describes performance of the proposed design using Microwind3.5 and DSCH 3.5 tool on 65nm technology. The simulated output of 4-bit ALU as shown in following figures

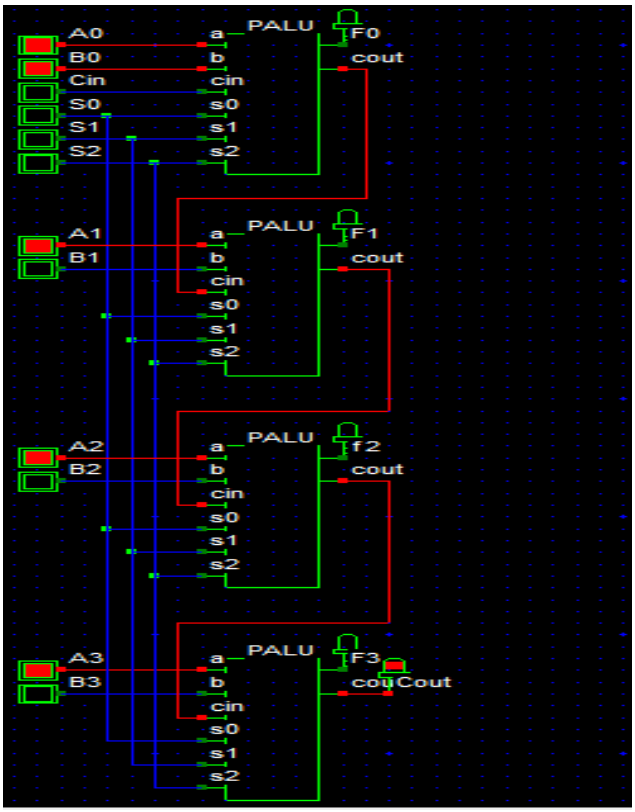

Fig 11. Schematic of 4-Bit ALU

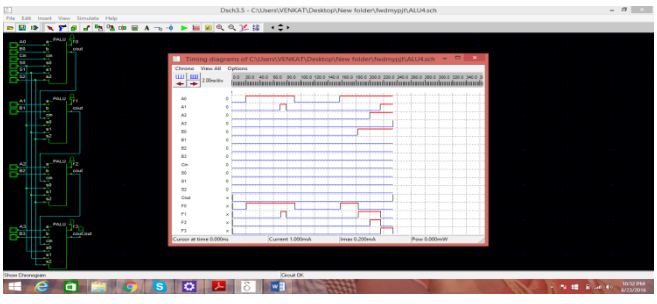

Fig 12. Timing Diagram of 4-Bit ALU

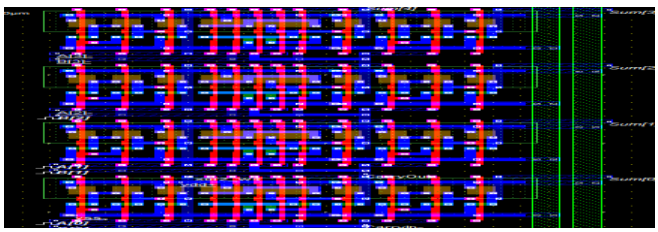

Fig 13. Layout of 4-Bit ALU

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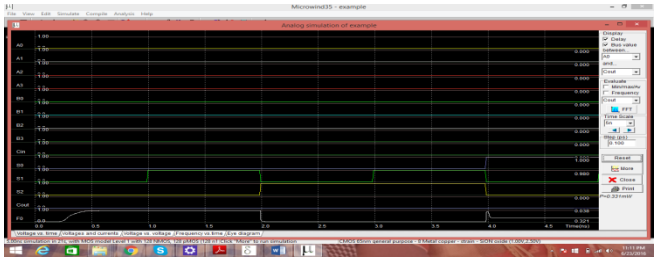

Fig 14. Simulated Output of 4-Bit ALU

TABLE III. ANALYSIS RESULT OF DIFFERENT BLOCK OF ALU

S.NO	DESIGN	CELL	POWER(uw)	No of Transistors
1	CMOS	2X1MUX	4.6	6
2		4X1MUX	15.1	18
3		Conventional 1Full Adder	16.6	28
4	GDI	2X1MUX	1.9	2
5		4X1MUX	2.9	6
6		Proposed 1Full Adder	10.1	10

TABLE IV. POWER CONSUMPTION OF 4-BIT ALU

S.NO	DESIGN	No of Transistors	Power(uw)
1	ALU with CMOS	240	512.4
2	ALU with GDI	152	29.316

VI. CONCLUSION

In CMOS circuit Power consumption is classified in two sections: dynamic power dissipation and static power dissipation. In today's CMOS circuits static power dissipation is negligible as compared to dynamic power dissipation therefore it is not considered. Dynamic Power dissipation in a CMOS circuit is given by $P = CL(Vdd^2/2)fclk$. The power supply is directly connected to dynamic power. The numbers of power supply connections to ground are reduced in GDI implementation which will reduce the dynamic power consumption. This paper presents a 4-bit ALU designed in 65nm technology for low power, high speed and area minimization with GDI technique. Various topologies of multiplexer and full adder implementation is studied and compared. The 4x1 multiplexer, 2x1 multiplexer, 1-bit full adder with 10-transistors designed using GDI technique is preferred for minimum possible area and lowering power consumption. The number of transistors ,Power dissipation and propagation delay of ALU were compared using CMOS and GDI techniques. GDI technique proved to have most excellent result in terms of performance characteristics among all the design techniques.

VII. REFERENCES

[1]. R. Shalem, E. John, and L.K.John, "A novel low-power energy recovery full adder cell," in Proc. Great Lakes Symp. VLSI, Feb. 1999, pp.380–383.

[2]. A.Sharma, R Singh and R. Mehra, " Low Power TG Full Adder Design Using CMOS Nano Technology,"

[3]. L.Bisdounis, D.Gouvetas and O.Koufopavlou, "A comparative study of CMOS circuit design styles for lowpower high-speed VLSI circuits" Int. J. of Electronics, Vol.84, No.6, pp 599- 613,1998. Anu Gupta, Design Explorations of VLSI Arithmetic Circuits, Ph.D. Thesis, BITS,Pilani, India, 2003.

[4]. Saradindu Panda, N. Mohan Kumar, C.K. Sarkar., "Transistor Count Optimization of Conventional CMOS Full Adder & Optimization of Power and Delay of New Implementation of 18 Transistor Full Adder by Dual Threshold Node Design with Submicron Channel Length" in Computers and Devices for Communication, 2009. CODEC 2009. 4th International Conference on pp: I – 4

[5]. T. Vigneswaran, B. Mukundhan, and P. Subbarami Reddy," A Novel Low Power, High Speed 14 Transistor CMOS Full Adder Cell with 50% Improvement in Threshold Loss Problem" in World Academy of Science, Engineering and Technology 13 2006 pp: I-7.

[6]. T. Esther Rani, M. Asha Rani, Dr. Rameshwar rao, "AREA OPTIMIZED LOW POWER ARITHMETIC AND LOGIC UNIT" 978-1-4244-8679-3/11/$26.00 ©2011 IEEE.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

[7]. Manish Kumar, Md. Anwar Hussain, and L.L.K. Singh," Design of a Low Power High Speed ALU in 45nm Using GDI Technique and Its Pe rformance Comparison, CNC 2011, CCIS142, pp. 458–463, 2011.

[8]. Morgenshtein, A., Fish, A., Wagner, I.A.: Gate-Diffusion Input (GDI) – A Technique for Low Power Design of Digital Circuits: Analysis and Characterization. In: ISCAS 2002, USA (May 2002).

[9]. K.-H. Cheng and c.-S. Huang, "The novel efficient design of XORlXNOR function for adder applications," in Proc. o/the 6th IEEE International Conference on Electronics. Circuits and System,vo1. 1 ,pp.29-32, 1999 .

[10]. R.Zimmermannn and W.Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid-State Circuits, vol. 32, pp. 1079–1090, July 1997. Y.Jiang, Y.Wang, and J.Wu, "Comprehensive Power Evaluation of Full Adders," Florida Atlantic Univ., Boca Raton, Tech. Rep., 2000.

[11]. R.Uma and P. Dhavachelvan," Modified Gate Diffusion Input Technique: A New Technique for Enhancing Performance in Full Adder Circuits" 2nd International Conference on Communication, Computing & Security [ICCCS-2012].

[12]. R.uma, Vidya Vijayan, M. Mohanapriya, Sharon Paul, Area, Delay and Power Comparison of Adder Topologies

[13]. J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp. 68-73.