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A High Gain Input-Parallel Output-Series DC/DC Converter with Dual Coupled Inductors

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Abstract:

High voltage gain DC-DC converters are required in many industrial applications such as PV and fuel cell energy systems, high intensity discharge lamp(HID), DC back-up energy systems and electric vehicles. This paper presents a novel input-parallel output-series boost converter with dual coupled-inductors and a voltage multiplier module. On the one hand, the primary windings of two coupled-inductors are connected in parallel to share the input current and reduce the current ripple at the input. On the other hand, the proposed converter inherits the merits of interleaved series-connected output capacitors for high voltage gain, low output voltage ripple and low switch voltage stress. Moreover, the secondary sides of two coupled-inductors are connected in series to a regenerative capacitor by a diode for extending the voltage gain and balancing the primary-parallel currents. In addition, the active switches are turned on at zero-current and the reverse recovery problem of diodes is alleviated by reasonable leakage inductances of the coupled inductors. Besides, the energy of leakage inductances can be recycled. A prototype circuit rated 500W output power is implemented in the laboratory, and the experimental results shows satisfactory agreement with the theoretical analysis.

Index Term- ***High gain, dc-dc converter, input-paralleloutput-series, dual coupled-inductors.***

I.INTRODUCTION

Nowadays high voltage gain DC-DC converters are required in many industrial applications[1]-[7], For example, photovoltaic (PV) energy conversion systems and fuel-cell systems usually need high step-up and large input current dc-dc converters to boost low voltage (18–56V) to high voltage (200–400V) for the grid-connected inverters. High-intensity discharge lamp ballasts for automobile headlamps call for high voltage gain dc-dc converters to raise a battery voltage of 12V up to 100V at steady operation [8], [9]. Also, the low battery voltage of 48V needs to be converted to 380V in the front-end stage in some uninterruptible power supplies (UPS) and telecommunication systems by high step-up converters [10]-[11].Theoretically, a basic boost converter can provide infinite voltage gain with extremely high duty ratio. In practice, the voltage gain is limited by the parasitic elements of the power devices, inductor and capacitor. Moreover, the extremely high duty cycle operation may induce serious reverse-recovery problem of the rectifier diode and large current ripples which increase the conduction losses. On the other hand, the input current is usually large in high output voltage and high power conversion, but low-voltage-rated power devices with small on-resistances may not be selected since the voltage stress of the main switch and diode is respectively equivalent to the output voltage in the conventional boost converter.

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Many single switch topologies based on conventional boost converter had been presented for high step-up voltage gain [11]-[15]. The cascaded boost converter is also capable of providing high voltage gain without the penalty of extreme duty-cycle [16]. However, the voltage stress of the main switch is equal to the output voltage. In references[17]and[18], several switching-capacitor/switching inductor structures are proposed, and transformer less hybrid dc-dc converters with high voltage gain are derived by the use of structures integrated with classical single switch non-isolated PWM converters. They present the following advantage: the energy in the magnetic elements is low, which leads to weight, size and cost saving for the inductor, and less conduction losses. Another method for achieving high step-up gain is the use of the voltage-lift technique [19], showing the advantage that the voltage stress across the switch is low. However, several diode-capacitor stages are required when the conversion ratio is very large, which makes the circuit complex. In addition, the single switch may suffer high current for high power applications, which risks reducing its efficiency.

Another alternative single switch converters including forward, fly-back and tapped-inductor boost can achieve high conversion ratio by adjusting the turns ratio of the transformer [20]-[22], but these converters require large transformer turns ratio to achieve high voltage gain. In [23], an integrated boost-flyback converter is proposed to achieve high voltage gain, and the energy of a leakage inductor is recycled into the output during the switch-off period. Unfortunately, the input current is pulsed from the experimental results. In addition, it should be noticed that the low-level input voltages usually cause large input currents and current ripples to flow through the single switch for high step up and high power dc-dc conversion, which also leads to increasing conduction losses. Therefore, the single-switch topologies are not perfect candidates for high step up dc-dc conversion In order to handle high input currents and reduce current ripples, the three-state switching cell based on interleaved control is introduced in boost converters [24]. However, the voltage gain of conventional three-state switching boost converter is only determined by the duty ratio [18]-[25]. Moreover, the voltage stresses of the power devices are still equivalent to output voltage. Thus, the large duty ratios, high switch voltage stresses and serious output diode reverse recovery problem are still major challenges for high step-up and high power conversion with satisfactory efficiency. To solve above drawbacks, some three-state switching converters with high static gain employing diode-capacitor cells were presented [25]. However, several diode-capacitor cells are required to meet a very high step-up gain. Thus, other topologies using three state switching cell and coupled inductors are investigated in [26]-[31]. Reference [27] proposes an interleaved boost converter with coupled inductors and a voltage doubler rectifier in order to satisfy the high step-up applications and low input current ripple, in which the secondary sides of two coupled-inductors are connected in series. The winding-cross-coupled inductors and output diode reverse-recovery alleviation techniques are also introduced in an interleaved three-state switching DC–DC converters [32]-[33], which can get a considerably high voltage conversion ratio and improve the performance of the converter. In [34], an interleaved fly-back converter based on three-state switching cell for high step up and high power conversion is proposed. Although the converter can eliminate the main limitations of the standard fly-back, this circuit is a little complex and the input current ripples are large from the experimental results.

This paper proposes an input-parallel output-series boost converter with dual coupled inductors for high step up and high power applications. This configuration inherits the merits of high voltage gain, low output voltage ripple and low-voltage stress across the power switches. Moreover, the presented converter is able to turn on the active switches at zero-current and alleviate the reverse recovery problem of diodes by reasonable leakage inductances of the coupled inductors.

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II. TOPOLOGY AND OPERATIONPRINCIPLE OF THE PRESENTEDCONVERTER

The derivation procedure for the proposed topology is shown in Fig. 1. This circuit can be divided as two parts. These two segments are named a modified interleaved boost converter and a voltage doubler module using capacitor-diode and coupled inductor technologies. The basic boost converter topology is shown in Fig. 1(a) and Fig.1 (b) is another boost version with the same function in which the output diode is placed on the negative dc-link rail. Fig.1(c) is called a modified interleaved boost converter, which is an input-parallel and output-series configuration derived from two basic boost types. Therefore, this part based on interleaved control has several main functions: 1) it can obtain double voltage gain of conventional interleaved boost; 2) low output voltage ripple due to the interleaved series-connected capacitors; 3) low switch voltage stresses. Then the double independent inductors in the modified interleaved boost converter are separately replaced by the primary windings of coupled inductors which are employed as energy storage and filtering as shown in Fig.1 (d).

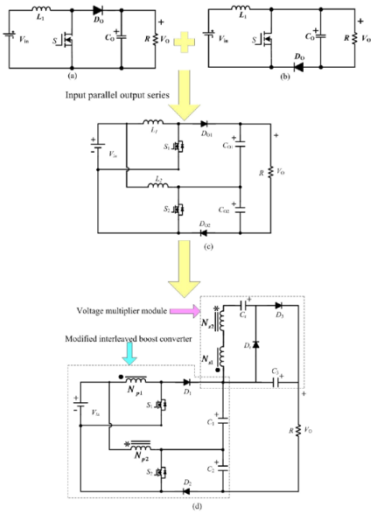

Fig. 1.The procedure to obtain the proposed converter with high voltage gain.(a) Conventional boost converter. (b) Other structure of boostconverter. (c) The modified interleaved boost. (d) A high gain input-parallel output-series DC/DC converter with dual coupled-inductos.

The secondary windings of two coupled inductors are connected in series for a voltage multiplier module, which is stacked on the output of the modified converter to get higher voltage gain. Fortunately, this connection is also helpful to balance the currents of two primary sides. The coupling references of the inductors are denoted by the marks "∗ " and "•". The equivalent circuit of the presented converter is demonstrated in Fig. 2,

L_{m1}, L_{m2}	magnetizing inductances
L_{k1}, L_{k2}	leakage inductances
C_1, C_2, C_3	output and clamp capacitors
S_1, S_2	main switches
D_1, D_2	clamp diodes
D_r, C_r	regenerative diode and capacitor
D_3	output diode
N	turns ratio of Ns /Np
V_{N1}, V_{N2}	the voltage on the primary sides of coupled inductors

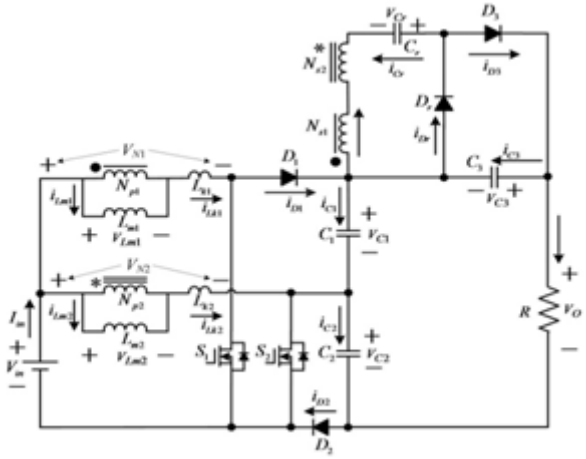

Fig. 2 The equivalent circuit of the presented converter

Fig. 3 shows the theoretical waveforms when the converter is operated in continuous conduction mode (CCM). The duty cycles of the power switches are interleaved with 180°phase shift, and the duty cycles are greater than 0.5. That is to say, the two switches can only be in one of three states (S1: on, S2: on; S1: on, S2: off; S1: off, S2: on;), which ensures the normal transmission of energy from the coupled inductor's primary side to the secondary one. The operating stages can be found in Fig.4- Fig.11.

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1)First stage [t0-t1]: At t = t0, the power switch S1 is turned on with zero current switching (ZCS) due to the leakage inductance Lk1, while S2 remains turned on, as shown in Fig. 4. Diodes D1, D2 and Dr are turned off, and only output diode D3 is conducting. The current falling rate through the output diode D3 is controlled by the leak-age inductances Lk1 and Lk2, which alleviates the diodes' reverse recovery problem. This stage ends when the current through the diode D3 decreases to zero.

2) Second stage [t1-t2]: During this interval, both the power switches S1 and S2 are maintained turned on, as shown in Fig.5 All of the diodes are reversed-biased. The magnetizing inductances Lm1 and Lm2 as well as leakage inductances Lk1 and Lk2 are linearly charged by the input voltage source Vin.

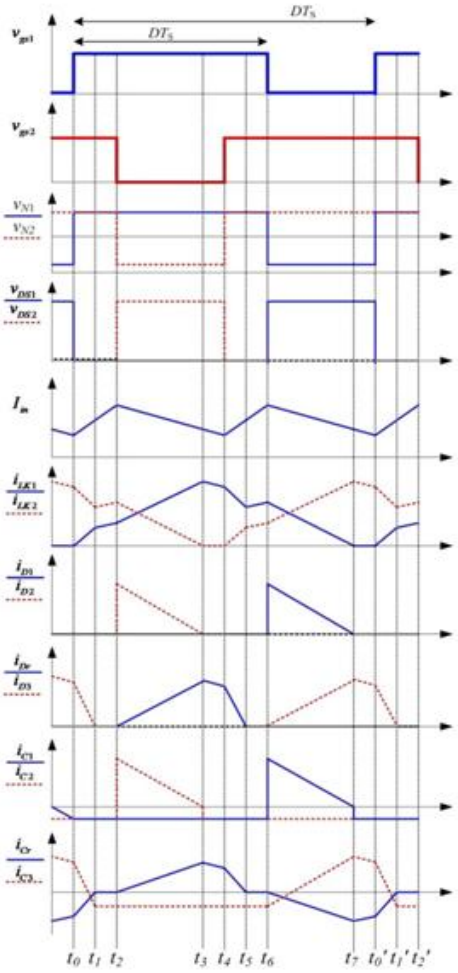

Fig. 3 Key theoretical waveforms

This period ends at the instant t2, when the switch S2 is turned off.

3)Third stage [t2-t3]: At t = t2, the switch S2 is turned off, which makes the diodes D2 and Dr turned on. The current flow path is shown in Fig. 6. The energy that magnetizing inductance Lm2 has stored is transferred to the secondary side charging the capacitor Cr by the diode Dr, and the current through the diode Dr and the capacitor Cr is determined by the leakage inductances Lk1 and Lk2. The input voltage source, magnetizing inductance Lm2 and leakage inductance Lk2 release energy to the capacitor C2 via diode D2.

4)Fourth stage [t3-t4]: At t = t3, diode D2 automatically switches off because the total energy of leakage inductance Lk2 has been completely released to the capacitor C2. There is no reverse recovery problem for the diode D2. The current-flow path of this stage is shown in Fig.7. Magnetizing inductance Lm2still transfers energy to the secondary side charging thecapacitor Cr via diode Dr. The current of the switch S1 is equal to the summation of the currents of the magnetizing inductances Lm1 and Lm2.

5)Fifth stage [t4-t5]: At t = t4, the switch S2 is turned on with ZCS soft-switching condition Due to the leakage inductance Lk2, and the switch S1remains in on state. The current-flowpath of this stage is shown in Fig.8. The current falling rate through the diode Dr is controlled by the leakage inductances Lk1and Lk2, which alleviates the diode reverse recoveryproblem. This stage ends when the current through the diode Drdecreases to zero at t = t5.

6)Sixth stage [t5-t6]: The operating states of stages 6 and 2 are similar. During this interval, all diodes are turned off. The magnetizing inductances Lm1, Lm2, and the leakage inductances Lk1, Lk2are charged linearly by the input voltage. The voltagestress of D1 is the voltage on C1, and the voltage stress of D2 is the voltage on C2. The voltage stress of Dr is equivalent to the voltage on Cr, and the voltage stress of D3 is the output voltage minus the voltages on C1 and C2 and Cr.

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7) Seventh stage [t6-t7]: The power switch S1 is turned off at t = t6, which turns on D1and D3, and the switch S2remainsin conducting state. The current-flow path of this stage is shown in Fig.10. The input voltage source Vin, magnetizing inductance Lm1 and leakage inductance Lk1 release their energy to the capacitor C1 via the switch S2. Simultaneously, the energy stored in magnetizing inductor Lm1 is transferred to the secondary side. The current through the secondary sides in series flows to the capacitor C3 and load through the diode D3.

8) Eighth stage [t7-t0 ′]: At t = t7, since the total energy of leakage inductance Lk1 has been completely released to the capacitor C1, diode D1 automatically switches off. The current of the magnetizing inductance Lm1 is directly transferred to the output through the secondary side of coupled inductor and D4 until t0′.

It should be pointed out that the time periods of stages I, IV, V and VIII are much shorter than those shown in Fig.3, which were enlarged in order to clearly show the waveform variations.

III. STEADY-STATE PERFORMANCE ANALYSIS OF THEPROPOSED CONVERTER

To simplify the circuit performance analysis of the proposed converter in CCM, and the following conditions are assumed.

1) All of the power devices are ideal. That is to say, the on-state resistance RDS(ON) and all parasitic capacitors of the main switches are neglected, and the forward voltage drop of the diodes is ignored;

2)The coupling-coefficient k of each coupled-inductor is defined as Lm/(Lm+Lk). The turn ratio N of each coupled-inductor is equal to NS /NP;

3)The parameters of two coupled-inductors are considered to be the same, namely

Lm1 = Lm2 = Lm, Lk1 = Lk2 = Lk,

NS1/NP1= NS2/NP2=N, k 1= Lm1/(Lm1+Lk1)= k2=Lm2/(Lm2+Lk2)=k ;

4) Capacitors C1, C2, C3 and Cr are large enough. Thus, the voltages across these capacitors are considered as constant in one switching period.

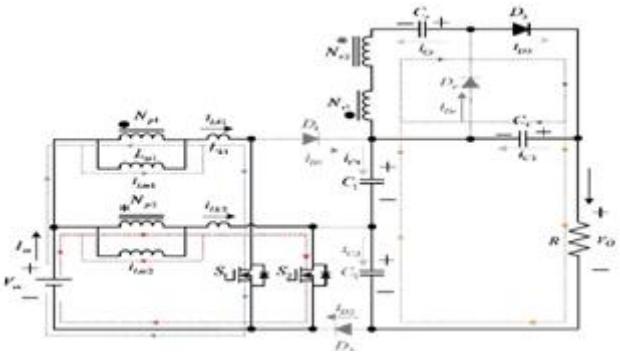

Fig. 4 First stage

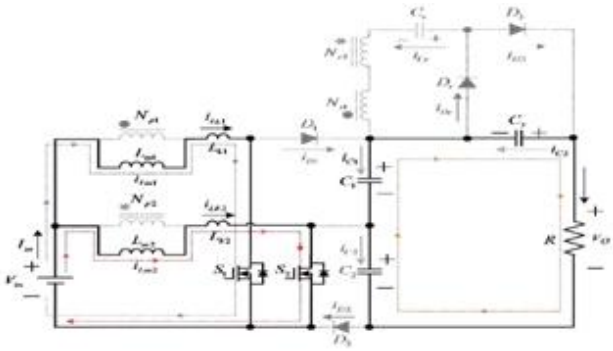

Fig. 5 Second stage

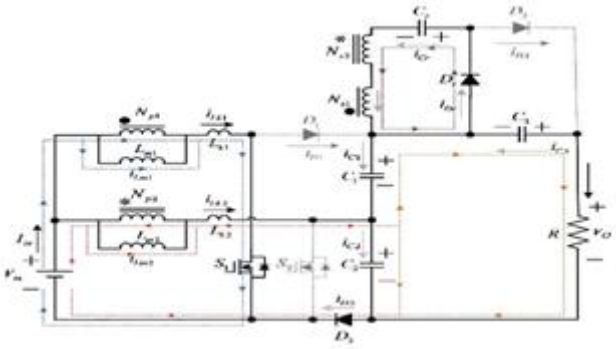

Fig. 6 Third stage

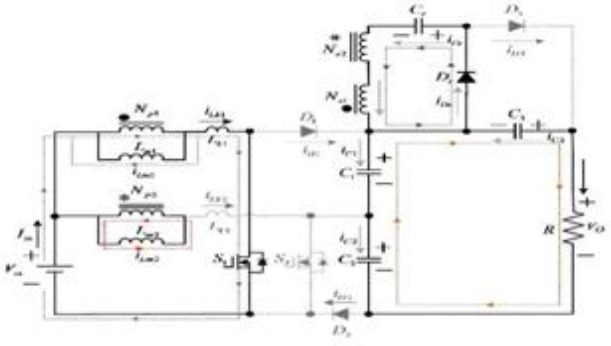

Fig. 7 Fourth stage

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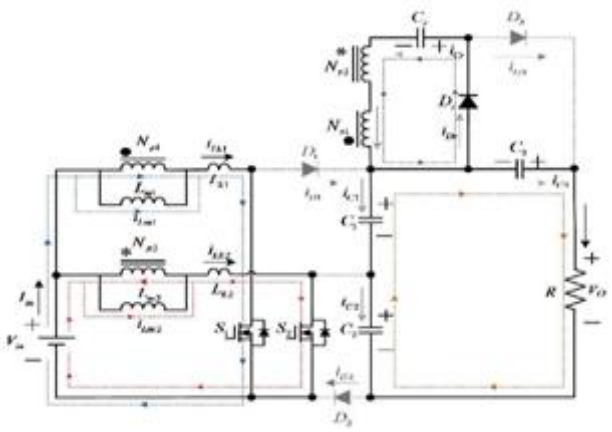

Fig. 8 Fifth stage

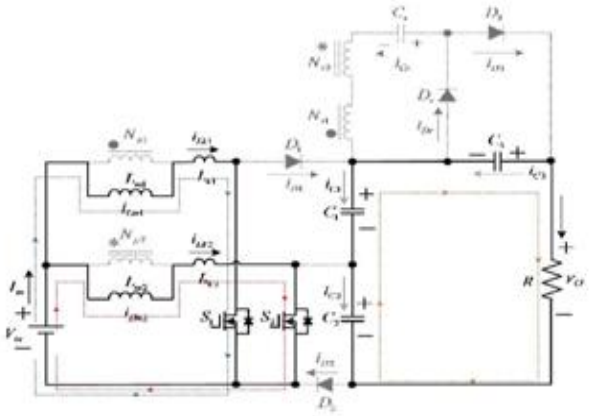

Fig. 9 Sixth stage

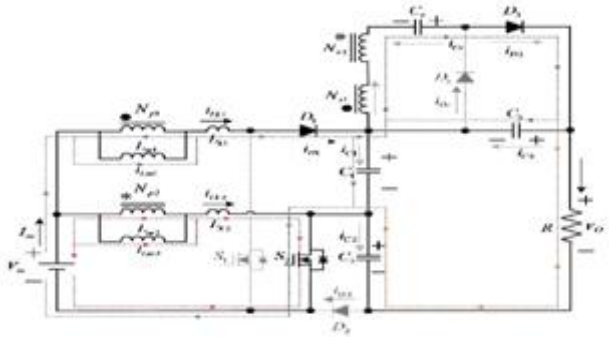

Fig. 10Seventh stage

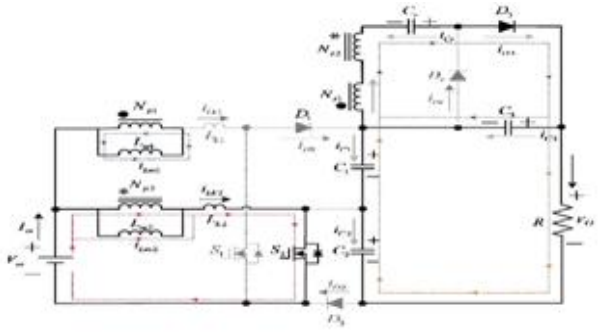

Fig. 11 Eighth stage

IV. DESIGN CONSIDERATIONS

A.Coupled Inductor Design

Usually, the duty cycle should be less than 0.8 to reduce conduction loss of the switches. If the voltage gainand switch duty cycle are selected, the turns ratio of the coupled inductor can be calculated. According to above analysis, the leakage inductance of the coupled inductors has some effects on the voltage gain. Fortunately, the leakage inductance can be used to limit the diode current falling rate and alleviate the diode reverse recovery problem. Therefore, a compromise should be made to optimize the performance of the converter. Moreover, considering the input current ripples and current sharing performance, the leakage inductance of the coupled inductors should be designed as symmetrical as possible. The relationship of the leakage inductance, the diode current falling rate,

B.Active Switches and Diodes Selection

The voltage -rating of the power components have been derived from (17)-(20). In practice, voltage spike may be produced during switch transition process because of the effect of the leakage inductance and parasitic capacitor. Therefore, regarding the margin of safety, the voltage -rating of the selected power devices will usually be more than 150% of the calculated value.

C.Considerations of Capacitor Design

How to suppress the voltage ripple on every capacitor an acceptable value is main consideration. According to Q C VCICT , The capacitance of the capacitors C1,C2, C3or Cr can be estimated by the equation (45)~(48),inwhich VO is the output voltage, VC1~ΔVC3 and VCr are the maximum tolerant voltage ripple on the capacitors C1, C2, C3 or Cr, and fS is the switching frequency, R is the loadGenerally, the equivalent series resistor (ESR) of an aluminum electrolytic capacitor will be smaller as the capacitance increases. So the capacitor is usually selected to be larger than the calculated value for reducing the power losses caused by the ESR. Moreover, it is a favorable

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solution that parallel several capacitors are adopted to make the equivalent ESR minimum.

V. EXPERIMENTAL VERIFICATIONS

In order to verify the operation and evaluate the performance of the proposed three-state switching boost converter with high voltage gain, a prototype was assembled and tested with the specifications defined in the Table II. Fig.14 shows some experimental current waveforms. Fig.14 (a) displays the gate signals of S1, the input current iin, the primary side leakage inductor currents iLK1 and iLK2 of the dual coupled inductors. It is seen that the currents iLK1, and iLK2 are nearly the same, which confirms the current sharing performance of the proposed converter. In addition, the input current ripples are very low due to the interleaved operation.Fig.14 (b) shows the gate signals of S1 and S2 and current waveforms passing through them. One can see that the active switches are turned on from zero current (ZCS), which reduces the switching losses and the EMI noise. Fig. 14(c) and(d) illustrate the experimental waveforms of iD1, iD2, iD3, and iDr, which agree with the operating principle and the steady-state analysis.

Table II Utilized components and parameters of prototype

Components	Parameters
Input voltage V_{in}	18-36V
Output voltage V_O	200V
Maximum output power P	500W
Switching frequency f_s	40kHz
Turns ratio N_s/N_p	19/18
Magnetizing inductor L_m	120uH
Leakage inductor L_{k1},L_{k2}	2.1 uH
Power switches S_1,S_2	FIRFP150N
Diodes D_1 ,D_3 and D_r	DSSK20-015A
Diode D_2	DSSK28-01AS
Capacitors C_1 and C_2	220uF/100 V
Capacitor C_r	47uF/100 V
Capacitor C_3	470uF/ 200V

Fig. 15 shows the voltage stress waveforms of main switches and diodes when turns ratio N is 1. From fig. 15.(a),it is seen that the voltage stresses Vds1and Vds2 on the main switches are only a quarter of the output voltage during the steady-state period, which is about 50 V. Thus low voltage ratings and low on-state resistance levels active switches can be selected for high efficiency. Fig. 15.(b) and (c) show that the voltage stresses on the diodes D1,D2,D3 and Dr. One can see that the voltage stresses of the diodes D1,D3 and Dr are approximately 100V which are equal to half of the output voltage in the steady-state period. The voltage stress of the diode D2 is only a quarter of the output voltage, approximately50V. Therefore, low-voltage rated Scotty diodes with high-performance can be adopted for the presented converter.

Fig. 16 shows the measured conversion efficiency of the proposed converter considering the loss of control circuit. The corresponding efficiency is around 94.37% at Po = 200 W. The full-load efficiency is appropriately 92.76%, In order to improve the efficiency further, the soft switching and integration magnetic techniques can be used to this converter, which is also the future work.

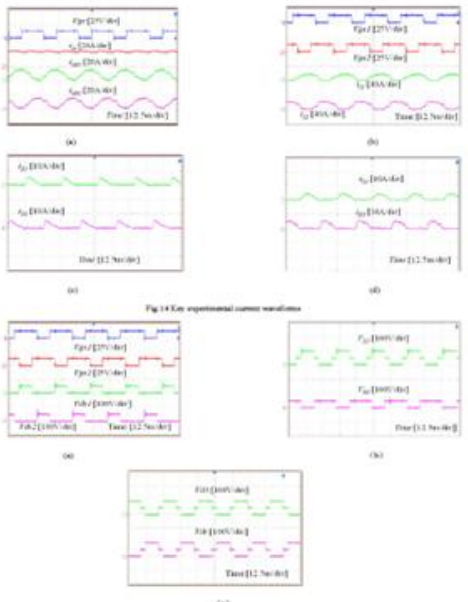

Fig. 15 The voltage stress waveforms of power components.

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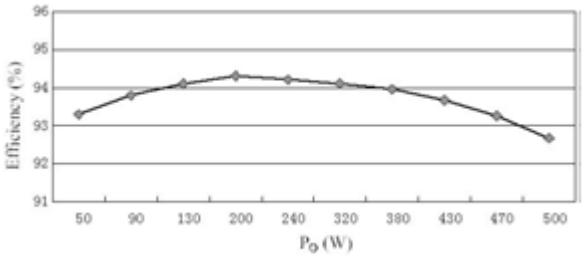

Fig.16. Measured efficiency of the proposed converter

VI. CONCLUSION

For low input-voltage and high step up power conversion, this paper has successfully developed a high-voltage gain dc-dc converter by input-parallel output-series and inductor techniques. The key theoretical waveforms, steady-state operational principle and the main circuit performance are discussed to explore the advantages of the proposed converter.

Some important characteristics of the proposed converter are: 1) It can achieve a much higher voltage gain and avoid operating at extreme duty cycle and numerous turn ratios; 2) the voltage stresses of the main switches are very low, which are one fourth of the output voltage under N=1; 3) The input current can be automatically shared by each phase and low ripple currents are obtained at input ; 4) the main switches can be turned on at ZCS so that the main switching losses are reduced; 5) The current falling rates of the diodes are controlled by the leakage inductance so that the diode reverse-recovery problem is alleviated. At the same time, there is a main disadvantage that the duty cycle of each switch shall be not less than 50% under the interleaved control with 180°phase shift.

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