ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Design & Implementation of a Low Power ALU Using GDI Technique

Pola Sudha Lakshmi
M.Tech (VLSI-SD),
Kshatriya College of Engineering.

Gopi Kondra, M.Tech (E.S,VLSI-SD),
Assistant Professor
Kshatriya College of Engineering.

Abstract

This paper proposes a new method for implementing a low power full adder and Arithmetic Logic Unit (ALU) by means of a set of Gate Diffusion Input (GDI) cell based logic gates and multiplexers. Full adder is a very common example of combinational circuits and is used widely in Application Specific Integrated Circuits (ASICs). An arithmetic logic unit (ALU) is a digital electronic circuit that performs arithmetic and bitwise logical operations on integer binary numbers. It is always advantageous to have low power action for the sub components used in VLSI chips. The explored technique of realization achieves a low power high speed design for a widely used subcomponent-full adder. This project can be extended to high speed Arithmetic Logic Unit (ALU). Simulated outcome using state-of-art simulation tool shows finer behavioural performance of the projected method over general CMOS based full adder. Power and area comparison between conventional and proposed full adder is also presented.

Keywords— ***Low power full adder, 2-Transistor GDI MUX, ASIC (Application Specific Integrated Circuit), 12-TFA, CMOS (Complementary Metal Oxide Semiconductor).***

INTRODUCTION

The binary addition is the basic arithmetic operation in digital circuits and it became essential in most of the digital systems including Arithmetic and Logic Unit (ALU), microprocessors and Digital Signal Processing (DSP). At present, the research continues on increasing the adder's delay performance.In many practical applications like mobile and telecommunications.With the tremendous progress of modern electronic system and the evolution of the nanotechnology, the low-power & high speed microelectronic devices has come to the forefront. Now a day, as growing applications (higher complexity), speed and portability are the major concerns of any smart device it demands small-size, low-power high throughput circuitry. So, sub-circuits of any VLSI chip needs high speed operation along with low-power consumption. Now a day logic circuits are designed using pass transistor logic techniques. In PTL based VLSI chips MOS switches are used to propagate different logic values in various node points, as it reduces area and delay as compared to any other switches type [1]. It reduces the number of MOS transistors used in circuit, but it suffers with a major problem that output voltage levels is no longer same as the input voltage level. Each transistor in series has a lower voltage at its output than at its input [2]. In order to minimize sneak paths, charge sharing, and switching delays of the circuit all the sub-circuit component has to be arranged obeying the VLSI design rules. Ensuring this simulation of circuit schematics provides a platform to verify circuit performance [3]. To get better speed and power consumption results lot of approaches have been recently proposed [4]-[7]. Among them, two have been established by Hitachi CPL [4] and DPL [6]. In 1993 Hitachi demonstrated a 1.5ns 32-bit ALU in 0.25μm CMOS technology [6] and 4.4ns 54X54 bit multiplier [7] using DPL technique. Like Pass Transistor Logic (PTL), Domino logic, NORA logic, Complementary Pass Logic (CPL), Differential Cascode Voltage Switch (DCVS), MOS Current Mode Logic (MCML), Clocked CMOS (C2MOS etc.[8][9] are also different approach for reducing the circuit power. In 2002, A. Morgenshtein, A. Fish, and Israel A. Wagner introduced a new method for low-power digital

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

combinational circuit design known as Gate Diffusion Input (GDI) [10]. The main purpose of this work is to implement a low power GDI based ALU& to draw a detailed comparative study with a CMOS full adder and 10T full adder.

The purpose of implementing the low power ALU is to show that using fewer number of transistors in comparison to the conventional full adder, conventional MUX, the power consumption and area gets reduced. It also helps in reducing the layout area thereby decreasing the entire size of a device where this adder is used. Power consumption is becoming the major tailback in the design of VLSI chips in modern process technologies. These are evaluated from an industrial product development perspective.

EXISTING DESIGN

The Full Adder circuit adds three one-bit binary numbers (a, b & c) and outputs two one-bit binary numbers, a sum (s) and a carry (co). The full adder is usually a component in cascade of adders, which add 4, 8, 16 etc. binary numbers.Implementation of full adder circuit using GDI techniquewhich is a basic building block of arithmetic and logic unit has been shown in Fig. 1.

While taking account of full adder the sum and carry outputs are represented as the following two combinational Boolean functions of the three input variables a, b and c.

Sum =axorb xor c ------- eqn.1

Carry = ab + ac + bc ------ eqn.2

Accordingly the functions can be represented by CMOS logic as follows in fig. 1,

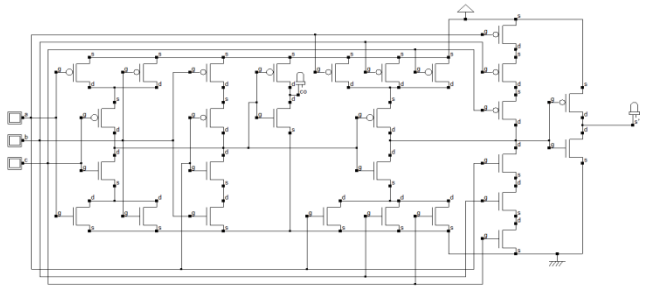

Fig. 1. Conventional 28-T CMOS 1 bit full adder

GDI technique based full adder have advantages over full adder using pass transistor logic or CMOS logic and is categorized by tremendous speed and low power. The technique has been described below.

Gate Diffusion Input (GDI)

Morgenshtein has proposed basic GDI cell shown in Fig.1 [8]. This is a new approach for designing low power digital combinational circuit.GDI technique is basically two transistor implementation of complex logic functions which provides in-cell swing restoration under certain operating condition. This approach leads to reduction in power consumption, propagation delay and area of digital circuits is obtained while having low complexity of logic design. An important feature of GDI cell is that the source of the PMOS in a GDI cell is not connected to VDD and the source of the NMOS is not connected to GND. Therefore GDI cell gives two extra input pins for use which makes the GDI design more flexible than CMOS design.

GDI Cell

Technique The GDI technique offers realization of extensive variety of logic functions using simple two transistor based circuit arrangement. This scheme is appropriate for fast and lowpower circuit design, which reduces number of MOS transistors as compared to CMOS and other existing low power techniques, while the logic level swing and static power dissipation improves. It also allows easy top-down approach by means of small cell library [5]. The basic cell of GDI is shown in Fig. 2.

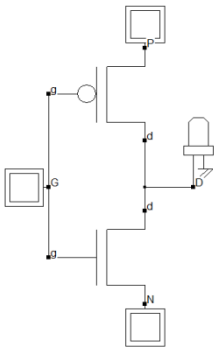

Fig 2 GDI basic cell consisting of pMOS and nMOS

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

1) The GDI cell consists of one nMOS and one pMOS. The structure looks like a CMOS inverter. Though in case of GDI both the sources and corresponding substrate terminals of transistors are not connected with supply and it can be randomly biased.
2) It has three input terminals: G (nMOS and pMOS shorted gate input), P (pMOS source input), and N (nMOS source input). The output is taken from D (nMOS and pMOS shorted drain terminal) [11].

GDI logic style approach consumes less silicon area compared to other logic styles as it consists of less transistor count. In view of the fact that, the area is less, the value of node capacitances will be less and for this reason GDI gates have faster operation which presents that GDI logic style is a power efficient method of design.
We can realize different Boolean functions with GDI basic cell. Table I shows how different Boolean functions can be realized by using different input arrangements of the GDI cell.

Table I. GDI Cell Based Various Logic Functions Using Different Input Configurations And Corresponding Transistor Counts

N	P	G	OUTPUT	FUNCTION	TRANSISTOR COUNT
0	1	A	A'	Inverter	2
0	B	A	A'B	F1	2
B	1	A	A'+B	F2	2
1	B	A	A+B	OR	2
B	0	A	AB	AND	2
C	B	A	A'B+AC	MUX	2
B'	B	A	A'B+B'A	XOR	4
B	B'	A	AB+A'B'	XNOR	4

ARCHITECTURE OF PROPOSED GDI FULL ADDER

MULTIPLEXOR:

Multiplexer is a digital switch. The multiplexer hasnumbers of input data lines and one output line. Theselection of a particular input line is controlled by a set ofselection line. There are '2n' input lines and 'n' selectionlines whose bit combinations determine which input is selected.The basic architecture of the 2:1 MUX using GDI method is shown in fig. 3. In this configuration we have connected PMOS and NMOS gate along with a SEL line 'A', as in MUX. As we know that PMOS works on ACTIVE LOW and NMOS works on ACTIVE HIGH. So, when the SELECT input is low (0) then the PMOS get activated, and show the input 'B' in the output and due to low input (0) the NMOS stands idle, as it is activated in high input.

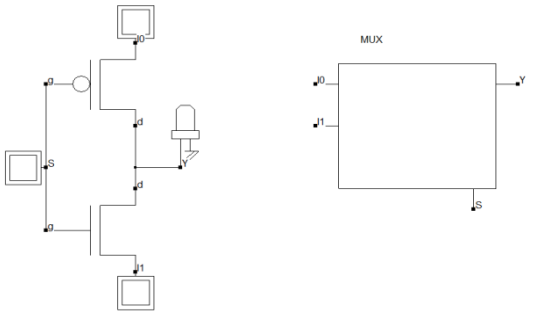

Fig.3 Basic view of 2T MUX using GDI technique

Same for the case, while the G input is high (1) then the NMOS get activated, and show the input 'C' at the output. Thus this circuitry behaves as a 2-input MUX using 'A' as SEL line, and shows the favorable output as 2:1MUX.

Similarly 4:1 MUX is shown below.

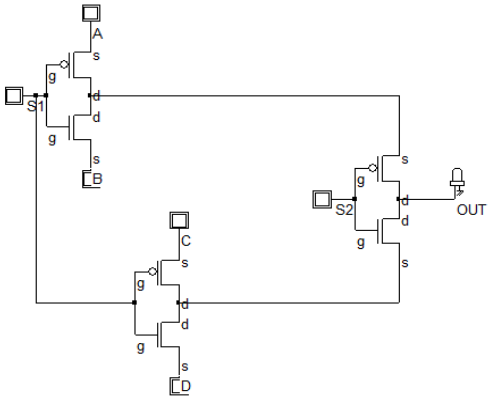

Fig 4: 4:1 MUX using GDI Technique

XOR Gate:

XOR gate is the main building block of full adder. The XOR gate using GDI technique is as shown in fig 5.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

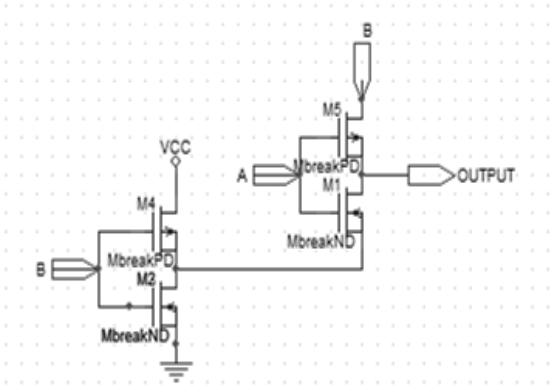

Fig5: XOR Gate using GDI Technique

FULL ADDER:

The 10T full adder is shown below.The Full Adder circuit adds three one-bit binary numbers(A, B & C) and outputs two one-bit binary numbers, a sum(S) and a carry (Cout). The full adder is usually a componentin cascade of adders, which add 4, 8, 16 etc. binary numbers.Implementation of full adder circuit using GDI 2:1 MUX takes 12 transistors by using GDI technique it takes only 10 transistors. The full adder is a basic building block of arithmetic and logic unit has been shown in Fig. 5.

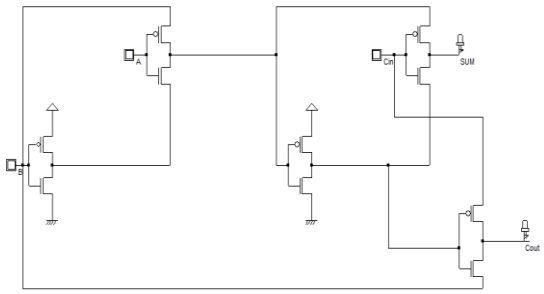

Fig 6: low power full adder using GDI technique

ARCHITECTURE OF AIRTHMETIC AND LOGIC UNIT

An arithmetic logic unit (ALU) is a fundamental building block of the Central Processing Unit (CPU) of a computer, and even the simplest microprocessors contain one. It is responsible for performing arithmetic and logic operations such as addition, subtraction, increment, decrement, logical AND, logical OR, logical XOR and logical XNOR.

ALU consists of eight 4x1 multiplexers, four 2x1 multiplexers and four full adders.When logic '1'and logic '0' are applied as an input INCREMENT and DECREMENT operations takes place respectively. An INCREMENT operation is analyzed as adding '1' to the addend and DECREMENT is seen as a subtraction operation [4]. Two's complement method is used for SUBTRACTION in which complement of B is used. The outputs obtained from the full adder are SUM, EXOR, EXNOR, AND & OR. Fig. 6 shows the block diagram of 4-bit ALU where first stage to fourth stage is cascaded with the CARRY bit.

The multiplexer stage selects the appropriate inputs based on the condition of the select signals, and gives it to the full adder which then computes the results. The multiplexer at the output stage selects the appropriate output and route it to output port. Table II shows the truth table for the operations performed by the ALU based on the status of the select signal. The operation being performed and the inputs andoutputs being selected are determined by set of three select signals incorporated in the design. Fig 9.shows multiplexer logic at input port and Fig10. shows multiplexer logic at output port. The multiplexer stage selects the appropriate inputs based on the condition of the select signals, and gives it to the full adder which then computes the results. The multiplexer at the output stage selects the appropriate output and route it to output port. Table 2 shows the truth table for the operations performed by the ALU based on the status of the select signal.

TABLE 2 OPERATION OF ALU

S2	S1	S0	Cin	FUNCTION	OPERATION
0	0	0	0	A+B	ADD
0	0	0	1	A+B+1	ADD WITH CARRY
0	0	1	0	A+B'	SUTRACT WITH BORROW
0	0	1	1	A-B	SUBTRACT
0	1	0	0	A	TRANSFER A
0	1	0	1	A+1	INCREMENT A BY 1
0	1	1	0	A-1	DECREMENT A BY 1
0	1	1	1	A	TRANSFER A
1	0	0	0	A&B	AND
1	0	1	0	A|B	OR
1	1	0	0	A^B	XOR
1	1	1	0	A'	COMPLEMENT

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

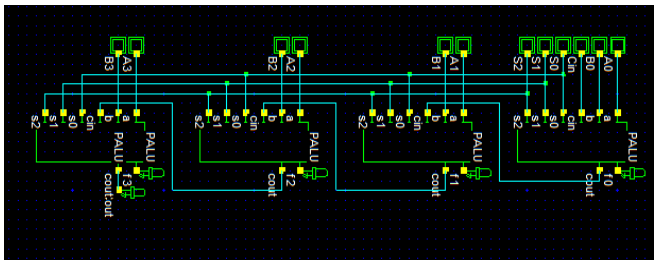

FIG 7: 4-bit ALU

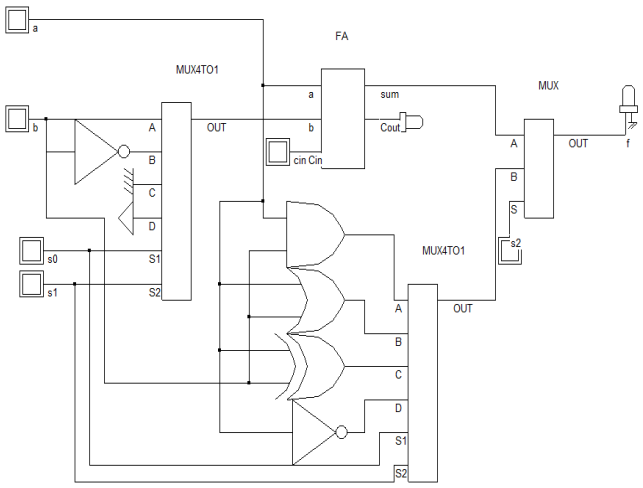

Fig8: 1-bit ALU

The cascading of four 1-bit ALU gives 4-bit ALU.

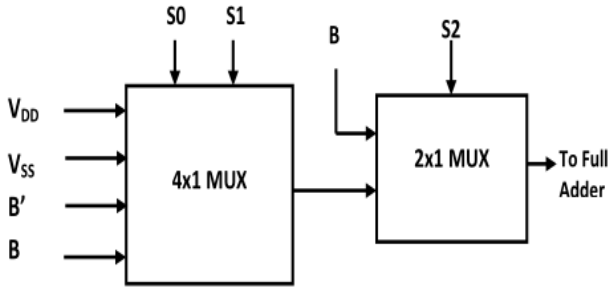

Fig 9:Block diagram of multiplexer at input stage

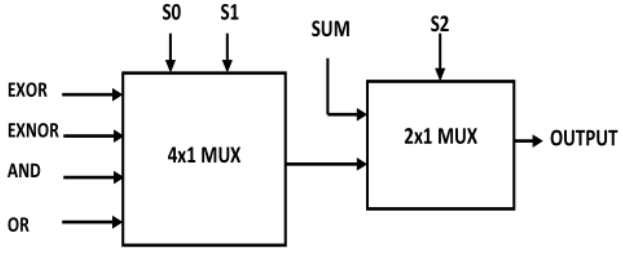

Fig10: Block diagram of multiplexer at output stage

SIMULATION RESULTS

All the simulations are performed on Microwind and DSCH 3.5. The main focus of this work is to meet all challenges faces in designing of ALUcircuit. The simulation results of full adder and ALU is shown below.

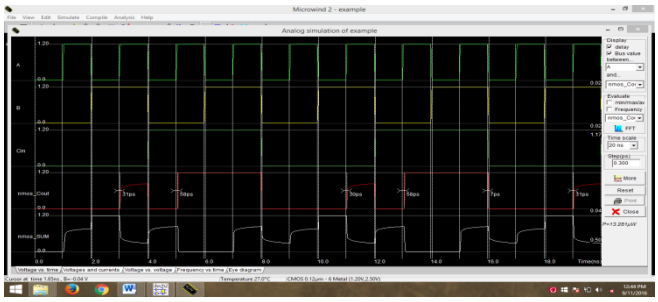

Fig11: simulation results of 10T full adder

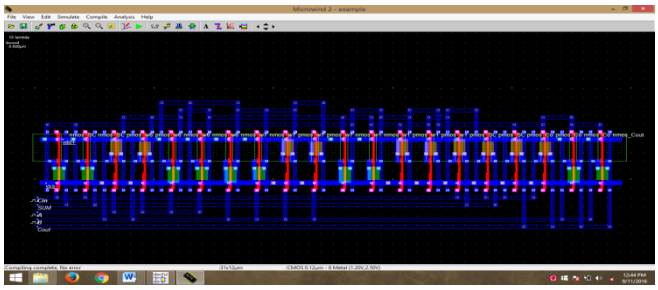

Fig 12: layout of 10T full adder

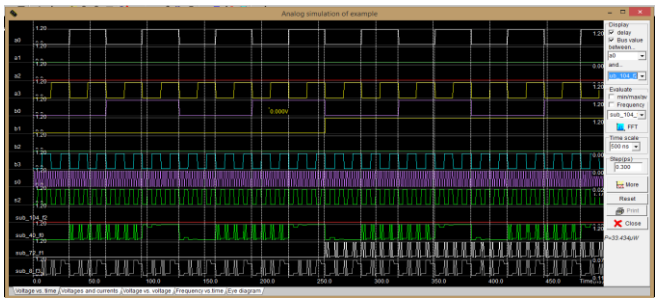

Fig 13: simulation results of ALU

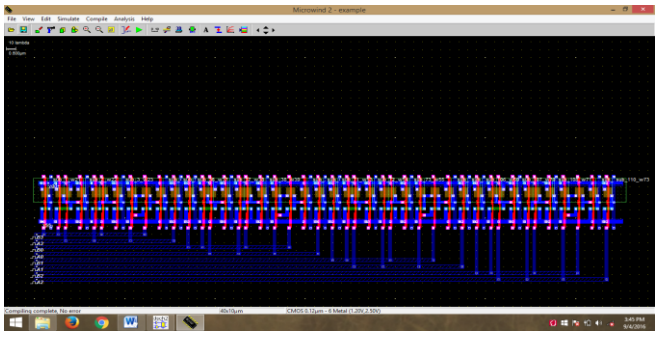

Fig 14: layout of ALU

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Table 3: Analysis result of different blocks of ALU

S. No.	Design	Cell	Power (µW)	No. of Trans-istor
1	CMOS	2x1 MUX	4.6073	6
2		4x1MUX	15.123	18
3		Conventiona l Full adder	16.675	28
4	Pass Transistor Gate	2x1 MUX	1.6079	4
5		4x1MUX	4.225	8
6		Full adder	11.998	24
7	GDI	2x1 MUX	1.394	2
8		4x1MUX	2.987	6
9		Full adder	10.190	10

CONCLUSION

Power consumption in CMOS circuit is classified in twocategorize: static power dissipation and dynamic powerdissipation. In today's CMOS circuits static powerdissipation is negligible thus not considered as compared todynamic power dissipation. Dynamic Power dissipation in aCMOS circuit is given by P = CLf VDD2. The power supplyis directly related to dynamic power. The numbers of powersupply to ground connections are reduced in GDIimplementation which reduces the dynamic powerconsumption.From the above results it can be concluded that our proposed full adder has got better performance in power and area consideration in comparison with conventional full adder. It shows that in contrast to other conventional techniques, this approach is better and it will be more appropriate for industrial practice in complex process technologies.

REFERENCES

[1] Jaume Segura, Charles F. Hawkins CMOS electronics: how it works, how it fails, Wiley-IEEE, 2004, page 132

[2] Clive Maxfield Bebop to the Boolean boogie: an unconventional guide to electronics Newnes, 2008, pp. 423-426

[3] Albert Raj/Latha VLSI Design PHI Learning Pvt. Ltd. pp. 150-153

[4] Yano, K, et al, "A 3.8 ns CMOS 16*16b multiplier using complementary pass transistor logic", IEEE J. Solid State Circuits, Vol 25, p388-395, April 1990

[5] Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha, and Jin-Gyun Chung, "A Novel Multiplexer-Based Low-Power Full Adder" IEEE Transaction on circuits and systems-II: Express Brief, Vol. 51, No. 7,p-345, July- 2004

[6] Makoto Suzuki, et al, "A 1.5 ns 32 b CMOS ALU in double pass transistor logic", ISSCC Dig. Tech. Papers, pp 90-91, February 1993.

[7] N. Ohkubo, et al, "A 4.4 ns CMOS 54X54 b multiplier using pass transistor multiplexer", Proceedings of the IEEE 1994 Custom Integrated Circuit Conference, May 1-4 1994, p599-602, San Diego, California.

[8] Mohamed W. Allam, "New Methodologies for Low-Power HighPerformance Digital VLSI Design", PhD. Thesis, University of Waterloo, Ontario, Canada, 2000

[9] A.Bazzazi and B. Eskafi, "Design and Implementation of Full Adder Cell with the GDI Technique Based on 0.18µm CMOS Technology", International MultiConference of Engineers and Computer Scientists (IMES) Vol II, March 17 - 19, 2010, Hong Kong

[10] ArkadiyMorgenshtein, Alexander Fish, and Israel A. Wagner, "GateDiffusion Input (GDI): A Power-Efficient Method for Digital Combinatorial Circuits", IEEE Transaction on VLSI Systems, Vol. 10

[11] Dan Wang. "Novel low power full adder cells in 180nm CMOS technology", 2009 4th IEEE Conference on Industrial Electronics and Applications, 05/2009