ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

A Novel High Step-Up Soften Switching Converter for Renewable Energy Applications

R.Lalitha
M.Tech,
Arjun College of Technology and Sciences.

Mr.Rosaiah Mudigondla, M.Tech
HOD,
Department of EEE,
Arjun College of Technology and Sciences.

Abstract:
In this paper, a novel high stride up DC/DC converter is displayed for Renewable Energy Applications. The recommended structure comprises of a coupled inductor and two voltage multiplier cells keeping in mind the end goal to get high stride up voltage pick up. Furthermore, two capacitors are charged amid the switch-off period utilizing the vitality put away as a part of the coupled inductor which expands the voltage exchange pick up. The vitality put away in the spillage inductance is reused with the utilization of a detached clasp circuit. The voltage weight on the primary force switch is likewise decreased in the proposed topology. In this manner, a fundamental force switch with low resistance RDS (ON)can be utilized to diminish the conduction misfortunes. The operation guideline and the consistent state investigations are examined completely. To confirm the execution of the displayed converter, a 300W research center model circuit is actualized. The outcomes approve the hypothetical examinations and the practicability of the exhibited high stride up converter.

Index Terms:
Coupled inductor, DC/DC converters, high step-up, switched capacitor**.**

I. INTRODUCTION:

Interest for spotless and supportable vitality sources has drastically expanded amid the previous couple of years with developing populace and modern advancement.

For quite a while, fossil fills have been utilized as the significant wellspring of producing electrical vitality. Natural results of these assets have made it important to profit by clean vitality sources, for example, wind and sun powered. Along these lines, conveyed era (DG) frameworks taking into account renewable vitality sources have pulled in the scientists' consideration. The DG frameworks incorporate photovoltaic (PV) cells, energy components and wind power [1]-[3].However, the yield voltages of these sources are not sufficiently huge for interfacing with air conditioning utility voltage. PV cells can be associated in arrangement with a specific end goal to acquire a huge dc voltage. Be that as it may, it is hard to overlook the shadow impact in PV boards [4]-[6]. High stride up converters are a reasonable answer for the previously mentioned issue. Each PV board can be associated with a specific high stride up converter. In this manner, every board can be controlled autonomously. These converters help the low information voltages (24-40 V) to a high voltage level 300-400 V) [7]. The fundamental elements of high stride up converters are their huge change proportion, high productivity and little size [8]-[10].Theoretically, conventional boost converters can achieve high voltage gain with an extremely high duty ratio [11]. However, the performance of the system will be deteriorated with a high duty cycle due to several problems such as low conversion efficiency, reverse-recovery and electromagnetic interference problems [12].

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Some transformer-based converters like forward, push-pull or fly back converters can accomplish high stride up voltage pick up by conforming the turn proportion of the transformer. In any case, the spillage inductor of the transformer will bring about significant issues, for example, voltage spike on the principle switch and high power scattering [13]. Keeping in mind the end goal to enhance the change productivity and get high stride up voltage increase, numerous converter structures have been introduced [14]-[29]. Exchanged capacitor [14]-[16] and voltage lift [17]-[19] strategies have been utilized broadly to accomplish high stride up voltage pick up. Be that as it may, in these structures, high charging streams will move through the primary switch and increment the conduction misfortunes Coupled-inductor based converters can likewise accomplish high stride up voltage pick up by changing the turn proportions [20], [21]. Be that as it may, the vitality put away in the spillage inductor causes a voltage spike on the fundamental switch and falls apart the conversion efficiency.

To conquer this issue, coupled-inductor based converters with a dynamic clasp circuit have been introduced in[22]. Some high stride up converters with two-switch [23]-[25] and single-switch [26]-[29] are presented in the late distributed writings. Be that as it may, the transformation proportion is not sufficiently expansive. This paper exhibits a novel high stride up DC/DC converter for renewable vitality applications. The proposed structure comprises of a coupled inductor and two voltage multiplier cells keeping in mind the end goal to acquire high stride up voltage pick up. Also, a capacitor is charged amid the switch-off period utilizing the vitality put away as a part of the coupled inductor which expands the voltage exchange pick up. The vitality put away in the spillage inductance is reused with the utilization of an inactive brace circuit. The voltage weight on the primary force switch is likewise lessened in the proposed topology. Thusly, a fundamental force switch with low resistance RDS (ON) can be utilized to lessen the conduction misfortunes. The operation rule and the unfaltering state investigations are examined altogether.

To check the execution of the displayed converter, a 300W research center model circuit is actualized. The outcomes accept the hypothetical investigations and the practicability of the exhibited high stride up converter.

II. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

The circuit arrangement of the proposed converter is appeared in Fig. 1. The proposed converter involves a DC info voltage (VI), dynamic force switch (S), coupled inductor, four diodes and four capacitors. Capacitor C1 and diode D1 are utilized as cinch circuit separately. The capacitor C3 is utilized as the capacitor of the augmented voltage multiplier cell. The capacitor C2 and diode D2 are the circuit components of the voltage multiplier which increment the voltage ofclamping capacitor C1. The coupled inductor is displayed as a perfect transformer with a turn proportion N (NP/NS), a polarizing inductor Lm and spillage inductor Lk.

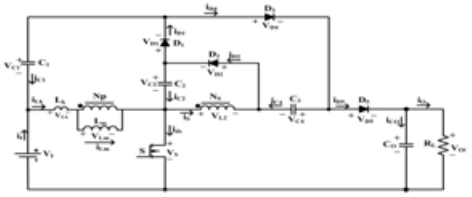


Fig. 1. Circuit configuration of the presented high step-up converter.

With a specific end goal to disentangle the circuit investigation of the converter, a few suppositions are considered as take after:

1) All Capacitors are adequately vast. In this way VC1, VC2, VC3, and VO are thought to be consistent amid one exchanging period.
2) All segments are perfect however the spillage inductance of the coupled inductor is considered.

As indicated by the previously mentioned presumptions, the CCM operation of the proposed converter incorporates five interims in one exchanging period. The present stream way of the proposed converter for every stage is delineated in Fig. 2.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Some common waveforms under persistent conduction mode (CCM) operation are represented in Fig. 3. The working stages are clarified as takes after.

Stage I [t0<t<t1 see Fig. 2(a)]: In this stage, switch S isturned on. Likewise, diodes D2 and D4 are turned on and diodes D1, D3 are killed. The DC source (VI) polarizes Lm through S. The auxiliary side of the coupled inductor is in parallel with capacitor C2 utilizing diode D2. As the current of the spillage inductor Lk increments straightly, the optional side current of the coupled inductor (iS) declines directly. The required vitality of burden (RL) is supplied by the yield capacitor CO. This interim finishes when the optional side current of the coupled inductor gets to be zero at t=t1.Stage II [t_1<t<t_2 see Fig. 2(b)]: In this stage, switch Sand diode D3 are turned on and diodes D1, D2 and D4 are killed. The DC source VI charges Lm through switch S. In this way, the current of the spillage inductor Lk and polarizing inductor Lm increment directly. The capacitor C3 is charged by dc source VI, cinch capacitor and the auxiliary side of the coupled inductor. Yield capacitor CO supplies the requested vitality of the heap RL. This interim finishes when switch (S) is killed at t=t2.

Stage III [t_2<t<t_3 see Fig. 2(c)]: In this stage, switch S isturned off. Diodes D_1 and D_3 are turned on what's more, diodes D2 and D4 are killed. The cinch capacitor C1 is charged by the put away vitality in capacitor C2 and the energies of spillage inductor Lk and polarizing inductor Lm. The streams of the optional side of the coupled inductor (iS) and the spillage inductorare expanded and diminished individually. The capacitor C3 is still charged through D3. Yield capacitor CO supplies the vitality to stack RL. This interim finishes when iLk is equivalent toiLm at t=t3.

Stage IV [t_3<t<t_4 see Fig. 2(d)]: In this stage, S is turnedoff. Diodes D_1 and D_4 are turned on and diodes D_2 and D_3 are turned off. The clamp capacitor C_1 is charged by the capacitor C_2 and the energies of leakage inductor L_k and magnetizing inductor L_m. The currents of the leakage inductor L_k and magnetizing inductor L_m decrease linearly. Also, a part of the energy stored in L_m is transferred to the secondary side of the coupled inductor. The dc source V_I, capacitor C_3 and both sides of the coupled inductor charge output capacitor and provide energy to the load R_L. This interval ends when diode D_1 is turned off at t=t_4.

Stage V [t_4<t<t_5 see Fig. 2(e)]: what's more, diodes D2 and D4 are killed. The cinch capacitor C1 is charged by the put away vitality in capacitor C2 and the energies of spillage inductor Lk and polarizing inductor Lm. The streams of the optional side of the coupled inductor (iS) and the spillage inductorare expanded and diminished individually. The capacitor C3 is still charged through D3. Yield capacitor CO supplies the vitality to stack RL. This interim finishes when iLk is equivalent toiLm at t=t3.

III. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

A. CCM Operation

To simplify the steady-state analysis, only stages II, IV and V are considered since these stages are sufficiently large in comparison with stages I and III.

During stage II, L_k and L_m is charged by dc source V_I. Therefore, the following equation can be written according to Fig. 2(b):

$V_{Lm}=kV_I$ (1) (1)

Where k is the coupling coefficient of coupled inductor which equals to $L_m/(L_m+L_k)$. Capacitor C_3 is charged by clamp capacitor C_1, dc source (V_I) and the secondary-side of the coupled inductor. The voltage across the capacitor C_3 can be expressed by:

$V_{C3}= V_{C1}+(kn+1)V_I$ (2) (2)

Where n is the turn ratio of coupled inductor which is equal to N_S /N_P. As shown in Fig. 2(d), during stage IV, L_k and L_m demagnetize to the clamp capacitor C_1 with the help of capacitor C_2. Hence, the voltage across L_m can be written as:

$V_{Lm}= k (V_{C2}- V_{C1})$ (3) (3)

Also, the output voltage can be formulated based on Fig.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

2(d):

$V_O = V_I + V_{C3} + (kn+1)(V_{C1} - V_{C2})$ (4) (4)

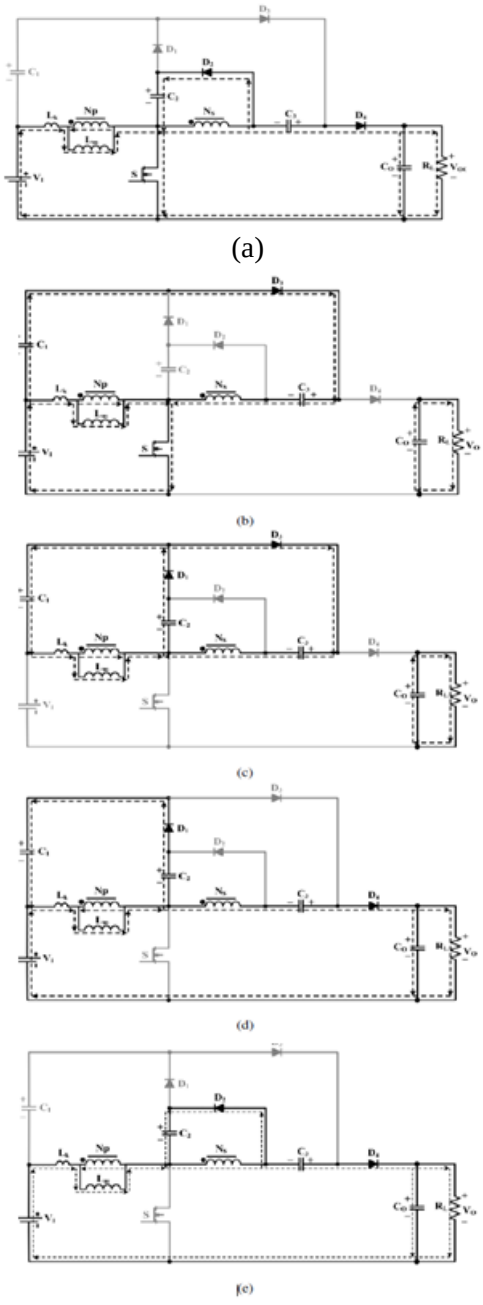


Fig. 2.Current-flow path of operating modes during one switching period at CCM operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode

According to Fig. 2(e), in the time interv al of stage V, the voltage across L_m can be expressed by:

$$\mathbf{V_{lm} = \frac{-V_{c2}}{n}} \quad \mathbf{(5)}$$

Moreover, the output voltage is derived as:

$$\mathbf{V_o = V_1 + V_{c3} + \left(\frac{1}{kn} + 1\right) V_{c2}} (6)$$

As indicated by previously mentioned supposition, the yield capacitor voltage is steady amid one exchanging period. In this way, by evening out of (4) and (6), the accompanying condition is inferred as:

$$\mathbf{V_{c1} = \left(\frac{kn+1}{kn}\right) V_{c2}} (7)$$

Utilizing the volt-second adjust guideline on Lm and conditions (1), (3), (5) and (7), the voltages crosswise over capacitors C1 and C2 is acquired as:

$$\mathbf{V_{c1} = \left(\frac{(kn+1)D}{1-D}\right) V_1} (8)$$

$$\mathbf{V_{c2} = \left(\frac{(kn)D}{1-D}\right) V_1} (9)$$

Substituting (8) into (2), yields:

$$\mathbf{V_{c3} = \left(\frac{(kn+1)D}{1-D}\right) V_1} \quad (10)$$

Substituting (9) and (10) into (6), the voltage gain is achieved as:

$$M_{CCM} = \frac{2 + kn + knD}{1 - D} V_1 \quad (11)$$

Fig. 4 demonstrates the varieties of the voltage pick up versus the obligation proportion with various coupling coefficients of the coupled inductor. It can be seen that the coupling coefficient is not exceptionally viable on the voltage pick up. At the point when k squares with 1, the perfect voltage increase is gotten as:

$$M_{CCM} = \frac{2 + n + nD}{1 - D} V_1 \quad (12)$$

The voltage pick up versus obligation proportion of the proposed converter and the converters proposed in [25], [29] and [30] under CCM operation with k=1 and n=2 are portrayed in Fig. 5.As it is indicated n Fig. 5 the proposed converter has higher voltage move pick up in examination with other con verters. Likewise, the voltage exchange increase of the introduced converter

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

is higher than the converter displayed in [27]. Nonetheless, in correlation with the introduced converter, an extra diode, an additional capacitor and a multi-winding coupled inductor is used in the converter displayed in [27].

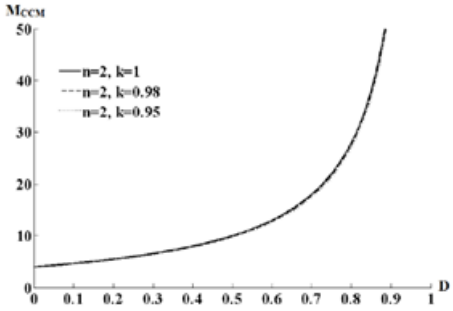


Fig. 4.Voltage gain versus duty ratio under various coupling coefficients of the coupled inductor.

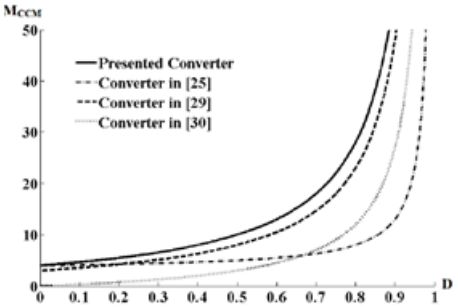


Fig. 5. Voltage gain versus duty ratio of the proposed converter, the converters in [25], [29] and [30] at CCM.

Based on the description of the operating modes, the voltage stresses on the active switch S and diodes D_1, D_2, D_3, and D_4 are expressed as:

$$V_{DS} = V_{D1} = \frac{1}{1-D} V_I = \frac{1}{2+2n}(V_O + nV_I) \quad (13)$$

$$V_{D2} = \frac{n}{1-D} V_I = \frac{n}{2+2n}(V_O + nV_I) \quad (14)$$

$$V_{D3} = V_{D4} = \frac{1+n}{1-D} V_I = \frac{1}{2}(V_O + nV_I) \quad (15)$$

According to Fig. 2, the average value of input current can be achieved as follows when switch is turned on/off:

$$I_{in(on)} = (n+1) I_{D3} + I_{Lm} \quad (16)$$

$$I_{in(off)} = I_O \quad (17)$$

From (16) and (17), the average current value of magnetizing inductor can be obtained as follow:

$$I_{Lm} = \frac{(M_{CCM} - 2 - n) I_O}{D} = \frac{2(n+1)}{1-D} I_O \quad (18)$$

The integral form of the current equation of magnetizing inductor can be written as:

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{1}{L_m} \int_{t_0}^{t} v_{Lm}(\tau) d\tau \quad (19)$$

the peak value of diode D_2 is obtained as:

$$i_{D2(peak)} = \frac{2(n+1) I_O}{n(1-D)}$$

B. Boundary Conduction mode (BCM) Operation

Similar to the analysis done in the former section, the voltage conversion ratio of the presented converter in discontinuous conduction mode (DCM) ca n be obtained as follows:

$$M_{DCM} = \frac{V_O}{V_I} = \frac{n + 2 + \sqrt{(n+2)^2 + \frac{D^2}{\tau_{Lm}}}}{2}$$

Fig. 6 demonstrates the bend of τLmB. On the off chance that τLmis bigger than τLmB, the proposed converter is worked under CCM. Fig. 7 demonstrates the Comparison of τLmB of the gaveconverte r converters in [28], [29] regarding the obligation cycle annd the change proportion. As it is appeared in Fig. 7, the CC M area of the exhibited converter is more extensive. Likewise, the CCM area of the exhibited converter is more extensive than the converter displayed in [27]. Subsequently, the introduced converter re quires a smallermagnetizing inductance to guarantee the CCM operation of the converter.

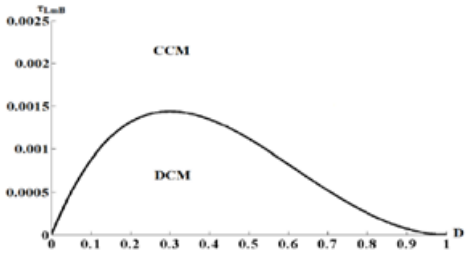
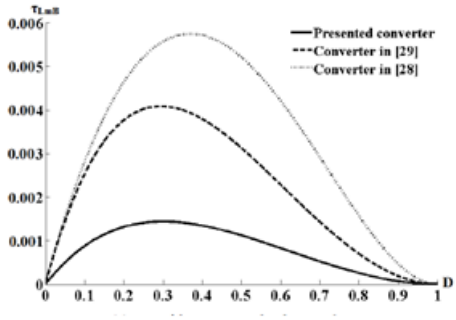
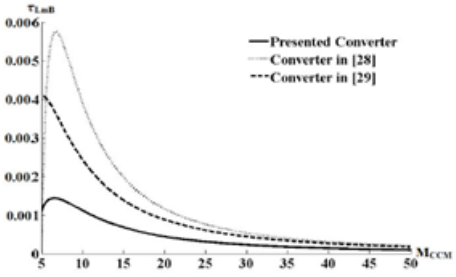


Fig. 6.Boundary condition of the proposed converter under n=2.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal



(a) τ_{LmB} with respect to th e duty cycle



(b) τ_{LmB} with respect to the conversion ratio.

Fig. 7.Comparison of τ_{LmB} of the presented converter with converters in [28], [29].

III. CAPACITORS AND INDUCTTANCE CALCULATION

The polarizing inductance of the coupled inductor is composed by and (29). To guarantee the CCM operation of the exhibited converter, the estimation of τLm must be more than τLm,B. In this way, the base estimation of the charging inductance can be ascertained as takes after:

$$L_{m_{min}} = \frac{D(1-D)^2 R_L}{8 f_S (n^2(1+D)+n(3+D)+1)}$$

As indicated by (30), the polarizing inductance ought to be more than 148μH. A coupled inductor with the charging inductance of the 300μH is utilized to ensure the CCM operation of the actualized converter. With a specific end goal to plan the extent of the capacitors, it ought to be taken after four conditions in regards to the swell in the yield voltage. The conditions are swell of the capacitor current, swell because of the proportionate arrangement resistance (ESR) of the capacitor, swell because of the comparable arrangement inductance (ESL) of the capacitor, and the hold-up time prerequisite for burden step reaction which the last condition is for the yield capacitor. To start with, the outline is begun by considering just the main condition which ESRs and ESLs are not known before selecting the capacitor. At that point, ESRs and ESLs are acquired from the capacitors' datasheets. The aggregate yield voltage swell is checked to ensure that it is beneath the allowable quality by considering ESRs and ESLs. What's more, the swell of the capacitor streams are ascertained and contrasted with the worth said in datasheet to ensure that the chose capacitors are in steady with the functional conditions. Keeping in mind the end goal to ascertain the voltage swell of a capacitor ESR and ESL, the accompanying condition is utilized.

$$V_C(t) = V_C(t_0) + \frac{1}{C}\int_{t_0}^{t} i(t)dt$$

Since the normal streams through capacitors C1, C2, C3 and CO are zero under enduring state, the normal current estimations of diodes are equivalent to IO. In this manner, as per the CCM operation modes appeared in Fig. 2 and (31), the voltage swell of all capacitors can be given as takes after:

$$\Delta V_{C1,2,3} = \frac{V_o}{R_L C} \quad , \quad \Delta V_{CO} = \frac{DV_o}{R_L C_O f_S}$$

The peak to- peak voltages across the capacitors' ESR are expressed below:

$$\Delta V_{C1}^{ESR} = r_{C1}\left(\left(\frac{4+n+(n-2)D}{D(1-D)}\right)I_O + \frac{DV_{in}}{L_m f_S}\right)$$

$$\Delta V_{C2}^{ESR} = r_{C2}\left(\left(\frac{2+n+nD+\frac{2D(n+1)}{n}}{D(1-D)}\right)I_O + \frac{DV_{in}}{L_m f_S}\right)$$

$$\Delta V_{C3}^{ESR} = r_{C3}\frac{2I_O}{D(1-D)}$$

$$\Delta V_{CO}^{ESR} = r_{CO}\frac{2I_O}{1-D}$$

The peak to- peak voltages across ESL of the capacitors are expressed below:

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

$$\Delta V_{C1}^{ESL} = L_{C1}\left(\frac{(n+1)\left(\left(\frac{2+n+nD}{D(1-D)}\right)I_O+\frac{DV_{in}}{L_m f_S}\right)}{(1-D)T_S}+\frac{2I_O}{D^2T_S}\right)$$

$$\Delta V_{C2}^{ESL} = L_{C2}\left(\frac{(n+1)\left(\left(\frac{2+n+nD}{D(1-D)}\right)I_O+\frac{DV_{in}}{L_m f_S}\right)}{(1-D)T_S}+\frac{2(n+1)^2 I_O}{n^2(1-D)^2T_S}\right)$$

$$\Delta V_{C3}^{ESL} = L_{C3}\left(\frac{2I_O}{(1-D)^2T_S}+\frac{2I_O}{D^2T_S}\right)$$

$$\Delta V_{CO}^{ESL} = L_{CO}\left(\frac{2I_O}{(1-D)^2T_S}\right)$$

The rms values of capacitor currents are as follows:

$$i_{C1rms} = \sqrt{\left(\left(\frac{2+n+nD}{D(1-D)}\right)I_o+\frac{DV_{in}}{L_m f_s}\right)\sqrt{\frac{3(1-D)}{1+n}}^2+\left(\frac{2I_o}{D}\sqrt{\frac{D}{3}}\right)^2}$$

$$i_{C2rms} = \sqrt{\left(\left(\frac{2+n+nD}{D(1-D)}\right)I_o+\frac{DV_{in}}{L_m f_s}\right)\sqrt{\frac{3(1-D)}{1+n}}^2+\left(\frac{2(n+1)I_o}{n(1-D)}\sqrt{\frac{3(1-D)n}{1+n}}\right)^2}$$

$$i_{C3rms} = I_O\sqrt{\left(\frac{2}{1-D}\sqrt{\frac{1-D}{3}}\right)^2+\left(\frac{2}{D}\sqrt{\frac{D}{3}}\right)^2}$$

$$i_{COrms} = I_O\sqrt{\frac{1+D^2}{3(1-D)}}$$

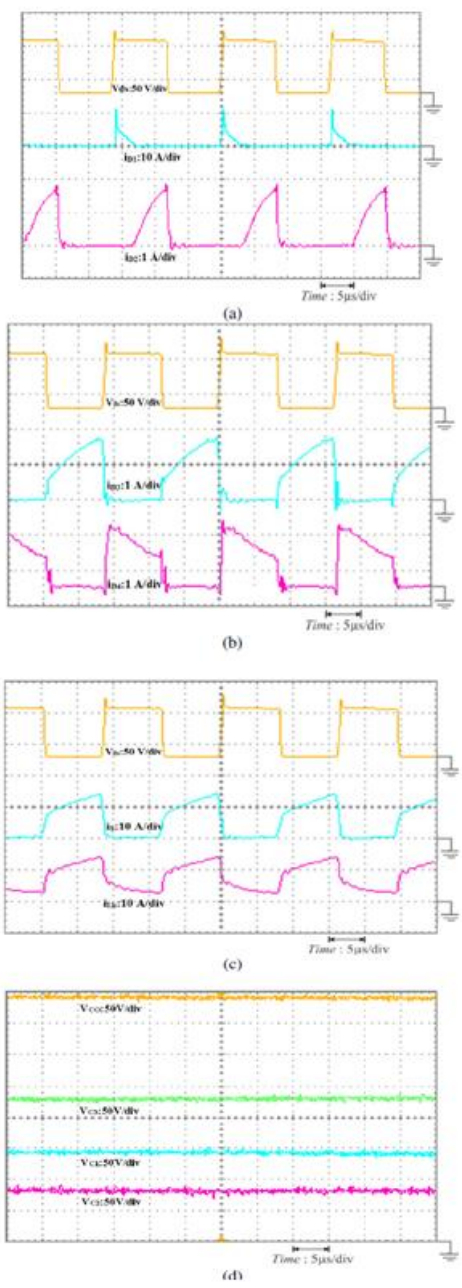
V. EXPERIMENTAL RESULTS

The execution of the exhibited converter is evaluated utilizing the model circuit actualized as a part of the research facility. The details of the executed circuit are given in Table 1. The trial results are appeared in Fig. 8 under burden 300W. The outcomes confirm the investigation of the consistent state operation. The voltage on the switch (VDS) amid the turn-off state is clasped to around 80V. Consequently, a low-voltage-evaluated switch can be utilized to enhance the productivity of the introduced converter. Fig. 8(a) demonstrates that the vitality put away in the spillage inductance is reused to capacitor C1 through diode D1. Fig. 8(e), (f) portray the voltage weights on the fundamental switch and diodes. Likewise, Fig. 8(d) demonstrates the voltages on capacitors C1, C2, C3 and CO which are in consistency with (8)- (11). The present waveforms of the diodes, switches and the coupled inductor (iLK) appeared in Fig. 8(a)- (c) accept the examination and the possibility of the proposed converter. The info current waveform with and without an information channel is additionally appeared in Fig. 8(g).The information current swell is as much as other proposed high stride up converters, for example, the converters in [27] - [29]. Be that as it may, as it is appeared in Fig. 8(g) (iSource), a low pass channel can be utilized to lessen the information current swell. The exploratory transformation productivity of the introduced converter is given in Fig. 9. The pinnacle estimation of productivity is 96.9% which is accomplished at PO=200W. The proficiency of the exhibited converter at full load PO=300W is 96%. The outcomes demonstrate the high transformation effectiveness of the introduced converter.

TABLE I: SPECIFICATIONS OF THE IMPLEMENTED PROTOTYPE

Specifications	Values
Input DC voltage	V_{in}=40 V
Output DC voltage	V_{out}=400 V
Switching frequency	F=60 kHz
Fast Diodes D_1, D_2, D_3, D_4	U1560
Coupled inductor	L_K: 1 µH, L_m: 300 µH
Capacitors C_1, C_2, C_3, C_o	47, 47, 100, 220 µF
Load	300 W
Power Switch (MOSFET)	IRFP260

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal



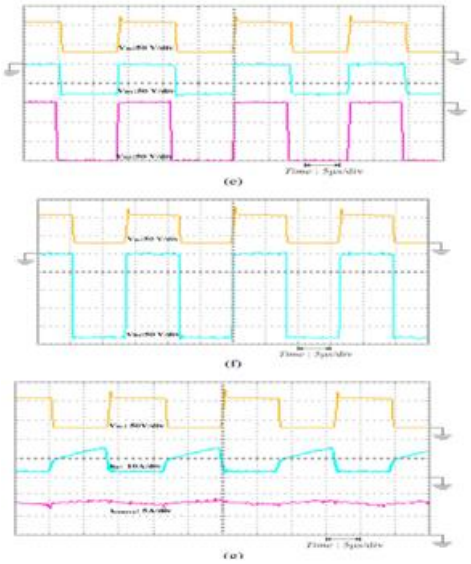


Fig. 8. Experimental results under load 300 W.

VI.CONCLUSION

This paper displays another high stride up DC/DC converter for Renewable Energy Applications. T he proposed converter is reasonable for DG frameworks in light of renewable vitality sources which require high stride up voltage exchange pick up. The vitality put away in the spillage inductance i s reused to enhance the execution of the displayed converter. Moreover, voltage weight on the fundamental force switch is lessened. Subsequently, a switch with a low on-state oppose ance can be picked. The consistent state operation of the converter has been broke down in point of interest. Additionally, the limit condition has been acquired. At long last, an equipment model is executed which changes over the 40-V information voltage into 400-V yield voltage. The outcomes demonstrate the achievability of the exhibited converter.

REFERENCES:

[1]F. Nejabatkhah, S. Danyali, S. Hosseini, M. Sabahi and S. Niapour, “Modeling and Control of a New Three-In put DC–DC Boost Converter for Hybrid PV/FC/Battery Power System,” IEEE Trans. Power Electron., vol. 27, no. 5, pp. 2309-2324, May. 2012.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

[2]R. J. Wai, and K. H. Jheng, "High-E fficiency Single-Input Multiple-Output DC–DC Converter," IEEE Trans. Po wer Electron., vol. 28, no. 2, pp. 886-898, Feb. 2013.

[3]Y. Zhao, X. Xiang, C. Li, Y. Gu,; W. Li, X. He, "Single-Phase High Step-up Converter With Improved Multiplier Cell Suitable for half- Bridge-Based PV Inverter System," IEEE Trans. Power Electron., vol. 29, no. 6, pp. 2807-2816, June 2014.

[4]J. H. Lee, T. J. Liang and J. F. Ch en, "Isolated Coupled-Inductor-Integrated DC–DC Converter With Non-dissipativeSnubber for Solar Energy Applications," IEEE Trans. Ind. Electron., v ol. 61, no. 7, pp. 3337-3348, Jul. 2014.

[5]C. Olalla, C. Delineand D. Maksimovic, "Performance of Mismatched PV Systems with Submodule Integrated Co nverters," IEEE Journal ofPhotovoltaic, vol. 4, no. 1, pp. 396-404, Jan. 2014.

[6]C. W. Chen, K. H. Chen, and Y. M. Chen, "Modeling and Controller Design of an Autonomous PV module for D MPPT PV Systems," IEEE Trans.Power Electron., vol. 29, no. 9, pp. 4723 - 47 32, Sept. 2014.

[7]Y. P. Hsieh, J. F. Chen, T. J. Liang, and L. S. Yang, "Analysis and implementation of a novel single-switch high step-up DC–DC converter," IETPower Electron., vol. 5, no. 1, pp. 11–21, Jan . 2012.

[8]Y. Zhao, W. Li, Y. Deng, and X.He, "H igh step-up boost converter with passive lossless clamp circuit for non-isolated high step-up applications," IETPower Electron., vol. 4, no. 8, pp. 851–859, Sept. 2011.

[9]I. Laird, and D. D. Lu, "High Step-U p DC/DC Topology and MPPT Algorithm for Use With a Thermoelectric Generator," IEEE Trans. PowerElectron., vol. 28, no. 7, pp. 3147-3157, Jul. 2013.

[10]R. J. Wai, C. Y. Lin, C. Y. Lin, R. Y. Duan, and Y. R. Chang, "High-efficiency power conversion system for kilowatt-level stand-alone generation unit with low input voltage," IEEE Trans. I nd. Electron., vol. 55, no. 10, pp. 3702–3714, Oct. 2008.

[11] L. S. Yang, T. J. Liang, and J. F. C hen, "Transformer-less DC–DC converter with high voltage gain," IEEE Tra ns. Ind. Electron., vol. 56, no. 8, pp. 3144–3152, Aug. 2009.

[12]Y. P. Hsieh, J. F. Chen, T. J. Liang, and L. S. Yang, "Novel High Step-Up DC–DC Converter With Coupled-Inductor and Switched-Capacitor Techniques," IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 998-1007, Feb. 2012.

[13]J. A. Carr, D. Hotz, J. C. Balda, H. A. Mantooth, A. Ong, and A. Agarwal, "Assessing the impact of SiC MO SFETs on converter interfaces for distributed energy resources," IEEE Trans. Power Electron., vol. 24, no. 1, pp. 260–270, Jan. 2009.

[14]C. L. Wei, and M. H. Shih, "Design of a Switched-Capacitor DC-DC Converter With a Wide Input Voltage Ra nge," IEEE Trans. Circuits andSystems, vol. 60, no. 6, pp. 1648-1656, Jun. 2 013.

[15]W. Qian, D. Cao, J. G. C. Rivera, M. Gebben, D. Wey, and F. Z. Peng, "A Switched-Capacitor DC–DC Converter With High Voltage Gain and Reduced Component Rating and Count," IE EE Trans. Ind. Electron., vol. 48, no. 4, pp. 1397-1406, Jul. 2012.