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MAC Design Using Vedic Multiplier

S.Tulasi
M.Tech Student,
Godavari Institute of Engineering And Technology,
Rajahmundry, E.G.District, AP.

Ch. Rajesh Babu, M.Tech
Assistant Professor
Godavari Institute of Engineering And Technology,
Rajahmundry, E.G.District, AP.

ABSTRACT:

The design of Multiplier Accumulator Unit (MAC) using Vedic Multiplier is the Ancient Indian Vedic Mathematics technique that has been modified as per technology for improving the performance of mathematical computations. MAC is a part of Digital Signal Processor. The MAC operational speed depends on the speed of multiplier. The proposed MAC unit area is reduced by reducing the number of multiplication and addition operations in the multiplier unit. Multiplier design in this unit is based on Vedic Mathematics. Adder unit is designed by using reversible logic. By the use of this reversible logic technique, power consumption and dissipation is greatly reduced. In Vedic Mathematics, different methods are available for doing multiplication; among those Urdhva Tiryagbhyam is the best approach to do multiplication. Urdhva Tiryagbhyam is a general formula of multiplication applicable to all cases of multiplication. It enables parallel generation of partial products, eliminates unwanted multiplication steps.

Keywords: ***MAC, Vedic Mathematics, Urdhva Tiryagbhyam, reversible logic***

I.INTRODUCTION:

MAC is an inevitable component in number of digital signal processing (DSP) applications involving multiplications and/or accumulations. MAC is used for high performance DSP systems. The DSP applications include filtering, convolution, and many other computing methods. Many of digital signal processing methods use nonlinear functions such as discrete cosine transform or discrete wavelet transforms. These are basically accomplished by repetitive usage of multiplication and addition, speed of multiplication and addition calculates the execution performance and speed of the entire computation.

Multiplication and accumulate operations are necessary for digital filters. Therefore, the functions of the MAC unit performs high-speed filtering and other processing especially for DSP applications. MAC unit operates completely independently from the CPU, it can perform operations separately on the given data and thereby the load on the CPU is reduced. The application like communication systems which is based on DSP, require extremely quick processing of large amount of data. The Fast Fourier Transform (FFT) also requires addition and multiplication. A MAC unit has a multiplier and an accumulator which contains the sum of the previous products. The MAC inputs are taken from the memory location and given to the multiplier block.

II.VEDIC MULTIPLIER:

A. Vedic Mathematics

Vedic mathematics is an ancient mathematics technique, which was formulated by Sri Jagadguru Swami Bharati Krishna Tirthaji (1884 - 1960). After a research of many years, he developed sixteen mathematical formulae from Atharvana Veda. The sutras (aphorisms) covered every topic of Mathematics such as Arithmetic, Geometry, Trigonometry, Algebra, differential, integral, etc., The word “Vedic” is obtained from the word “Veda” which means the power house of entire knowledge and divine [2, 3]. The proposed Vedic multiplier is based on the “Urdhava Tiryagbhayam” sutra (algorithm). These Sutras are traditionally used for the multiplication of numbers in the decimal number system.

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In this work, we will use similar techniques to solve the binary number system to make the new aphorism, which will be more suitable for the digital systems. It is a general multiplication formula applicable to all cases of multiplication.

B . Urdhava Tiryagbhyam

It literally means vertically , crosswise operation. Shift operation is not needed because the partial product calculation will performs in a single step, which in turn saves time and power. This is the main advantage of the Vedic multiplier.

An example for the Urdhva Triyagbhayam sutra is as follows: 9284 * 5137

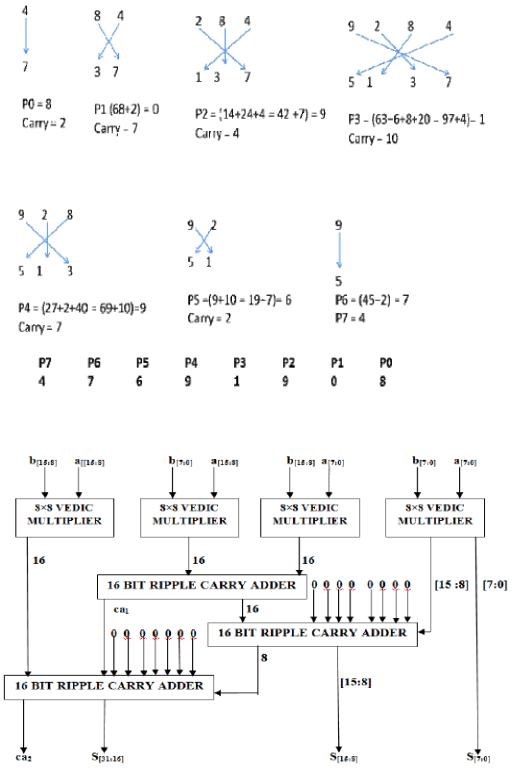

Fig1: 16×16 Vedic multiplier using 8×8 Vedic multiplier

In this method of vedic multiplier design , the adder block is designed by using the ripple carry adder. So, the major drawback in this design is larger delay why because the generation of previous carry is utilized for the generation of next stage carryout signal. So the vedic multiplier design using ripple carry adder has highest delay. This would be overcomed in the modified multiplier used in the MAC design.

III . MAC Unit

A multiplying process can be carried out in three steps: partial product Generation (PPG), partial product addition (PPA), and final addition. The two bottle necks should be considered that increasing the speed of MAC are reduction of partial product and accumulator block. The 32bit Mac design by using Vedic multiplier and reversible logic gate can be implement in two parts. First, multiplier , where a conventional multiplier is replaced by Vedic multiplier using Urdhava Tiryagbhayam sutra. Multiplication is the fundamental operation of MAC unit [1]. Power consumption, dissipation, speed, area and latency are the major issues in the multiplier unit. So, to avoid them, we go for fast multipliers in various applications of DSP, network techniques etc. There are two major criterions that improve the speed of the MAC units they are the partial products reduction and accumulator because of that burden is reduced. The second part is the Reversible logic gate. In recent VLSI, fast switching of signals leads to more power dissipation. That power dissipation is reduced by using this reversible logic approach. In recent years, reversible logic functions has emerged and played a crucial role in several fields such as Optical, Nano, Cryptography, etc.

A. MAC architecture:

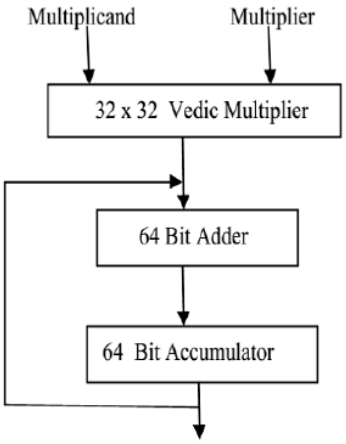

Fig 2: 32×32 MAC Architecture

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IV. MODIFIED MULTIPLIER:

32×32 Vedic Multiplier is designed by using 16×16 multiplier and adder blocks. We have modified the final adder stage with the Kogge stone adder which is more efficient than other adders which is shown in the fig3. Kogge stone adder is a parallel prefix adder which is one of the fastest adders. By using this Vedic multiplier we can achieve less partial products and adder stages as compared to the conventional multiplier. The multiplier design is simulated and synthesized using Xilinx.

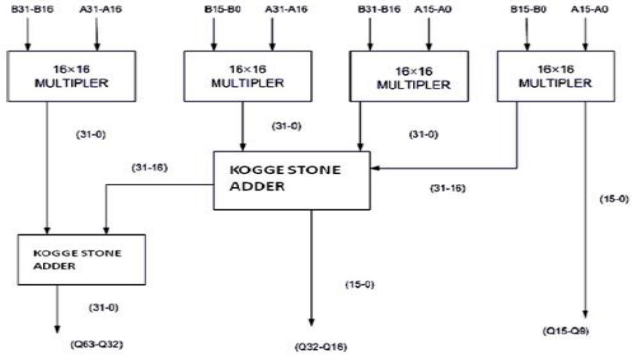

Fig 3:32 × 32 Vedic Multiplier with Kogge Stone Adder

V. ADDER USING REVERSIBLE LOGIC:

A. Reversible logic

Reversible logic is a unique technique. There is no loss of information occurred in this reversible logic. In this, the numbers of outputs are equal to the number of inputs.

General consideration for reversible logic gate:

- Fan-out is not permitted
- Feedbacks or loops are not permitted
- Garbage outputs are Minimum
- Minimum delay
- Minimum quantum cost
- Zero energy dissipation

A Boolean function is reversible if each value in the input set can be mapped with a unique value in the output set. Landauer [18] proved that the usage of traditional irreversible circuits leads to power dissipation and Bennet [17] showed that a circuit consisting of only reversible gates does not have power dissipate. In the design of reversible logic circuits, the following points must be kept in mind to achieve an optimized circuit:

B . DKG Gate

A 4*4 reversible DKG gate [6] that can work singly as a reversible full adder and a reversible full subtractor. If input A=0, the DKG gate acts as a reversible Full adder, and if input A=1 then it works as a reversible Full subtractor.

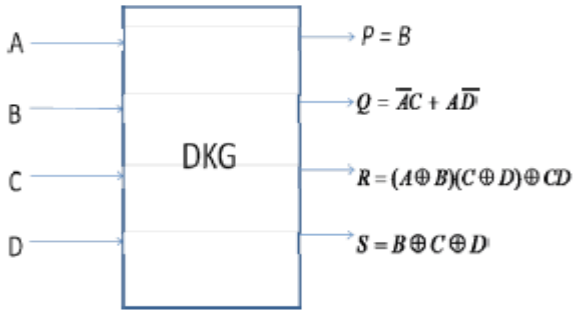

Fig4: DKG gate

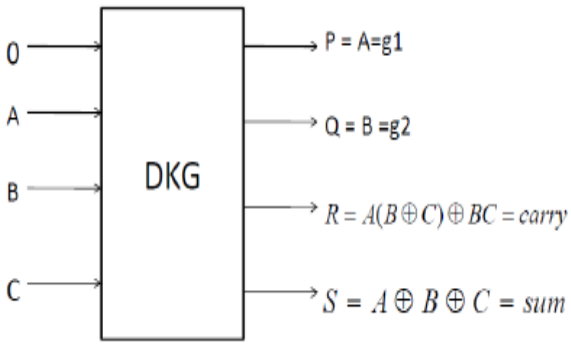

Fig5: DKG gate as a Full adder

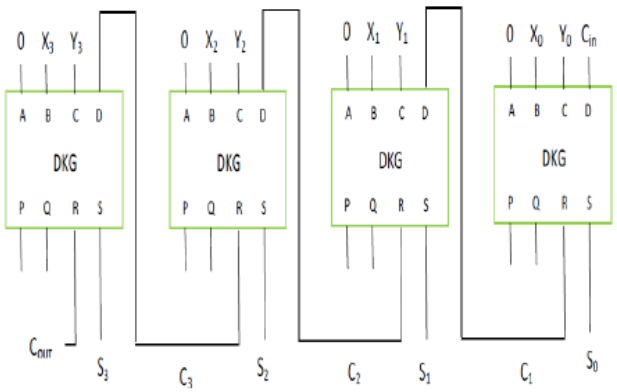

Fig6: Parallel adder using DKG gate

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VI. ACCUMULATOR STAGE:

Accumulator has an important role in the DSP applications in various ranges .The register designed in the accumulator has a special quality that it should add the multiplied numbers. Multiplier, adder and an accumulator are forming the essential foundation for the MAC unit. The accumulator block is enabled with a clock input. At every active clock input, the data in the accumulator is added with the present multiplier output. The process is highly essential for this today digital world.

The combination of Vedic Multiplier, Reversible Adder and an Accumulator blocks forms the efficient and high performance MAC unit.

VII. RESULTS:

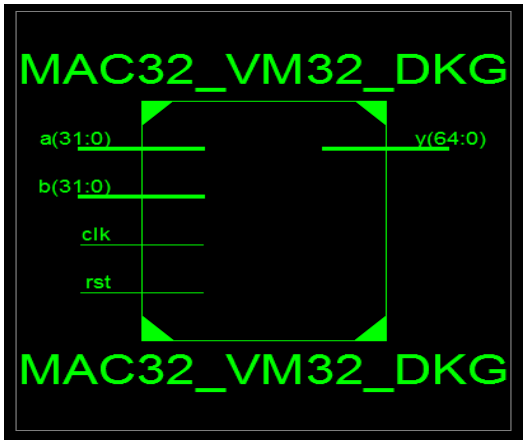

Fig7:RTL schematic of 32bit-MAC using 32x32 vedic multiplier with DKG Logic gate

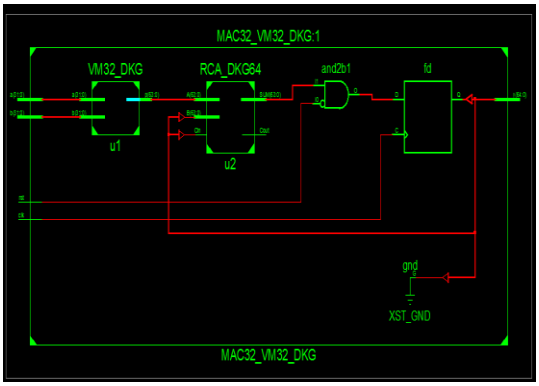

Fig8: RTL sub schematic of 32bit-MAC using 32x32 vedic multiplier with DKG Logic gate

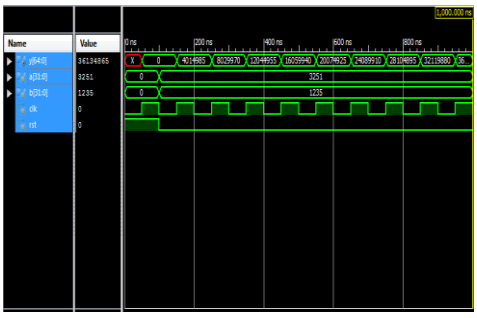

Fig9:Simulation of 32bit-MAC using 32x32 vedic multiplier with DKG Logic gate

VIII. CONCLUSION AND FUTURE SCOPE:

The results obtained by the design of Vedic multiplier and reversible logic designs are quite good. The work presented is based on 32bit MAC unit with Vedic Multipliers. We have designed basic building blocks of MAC unit and its performance has been analyzed for all the blocks. Therefore, we can say that the Urdhava Triyagbhayam sutra with 32-bit Multiplier and reversible logic is the best approach in all aspects like speed, delay, area and complexity as compared to other approaches. MAC unit is the basic block in different designs; hence researches are going on to reconfigure the MAC structure, especially using the recent emerging technology Reversible logic. Spectrum Analysis and Correlation linear filtering are the applications of transform algorithm further added to the field of communication, signal and image processing and instrumentation, and some other. Combining the Vedic and reversible logic will lead to new and efficient achievements in developing various fields of Mathematics, science as well as engineering.

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