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Efficient Implementation of Shift Register Using Pulsed Latches

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Abstract

Shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers, and image processing ICs. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. This paper proposes a low-power and area-efficient shift register using pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

INTRODUCTION

A SHIFT register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers, and image processing ICs. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register. A 16-megapixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.

It proposes a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

A master-slave flip-flop using two latches in Fig. 1 (a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1 (b).

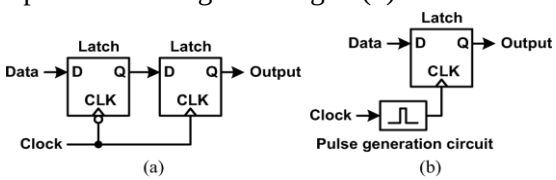

Fig.1 (a) Master-slave flip-flop (b) Pulsed latch

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All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop.

The pulsed latch is an attractive solution for small area and low power consumption. The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig.2.

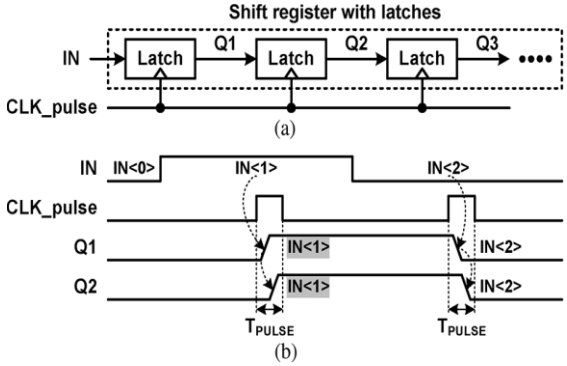


Fig: 2 Shift register with latches and a pulsed clock signal (a) Schematic (b) Waveforms

The shifts register in Fig. 2 (a) Consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. 2 (b) Show the timing problem in the shifter regi1ster. The output signal of the first latch (Q1) changes correctly because the input signals of the first latch (IN) is constant during the clock pulse width. But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

One solution for the timing problem is to add delay circuits between latches, as shown in Fig.3 (a). The output signal of the latch is delayed and reaches the next latch after the clock pulse.

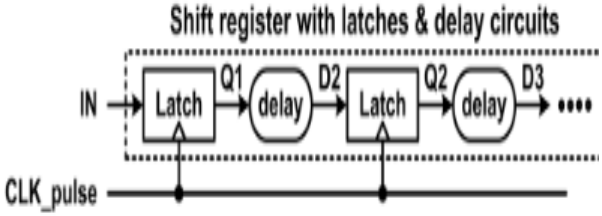
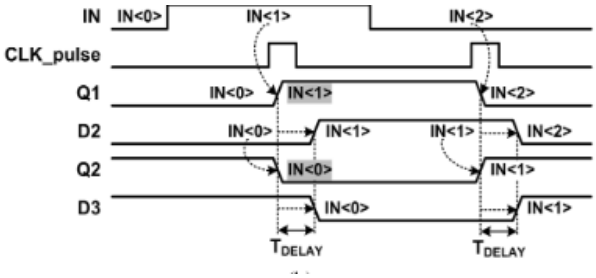


Fig.3. Shift register with latches, delay circuits (a) Schematic



(b) Waveforms.

The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in Fig. 3.(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problems occur between the latches. However, the delay circuits cause large area and power overheads.

Another solution is to use multiple non-overlaps delayed pulsed clock signals, as shown in Fig. 4 (a). The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits.

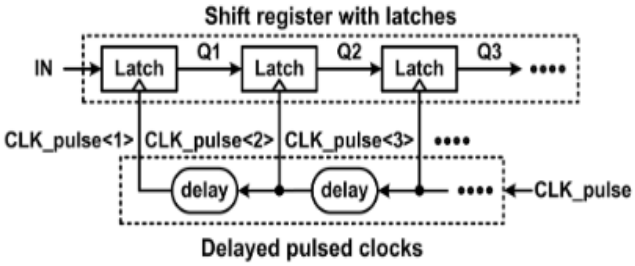
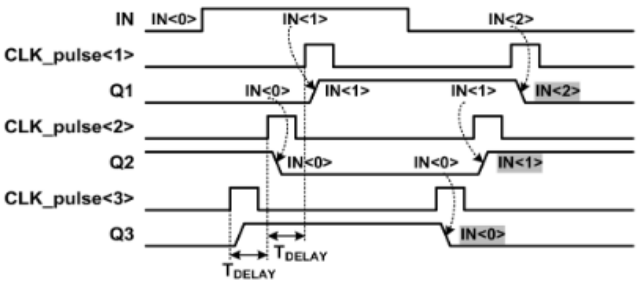


Fig.4 Shift register with latches and delayed pulsed clock signals (a) Schematic.



(b) Waveforms

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Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits.

Proposed Shift Register

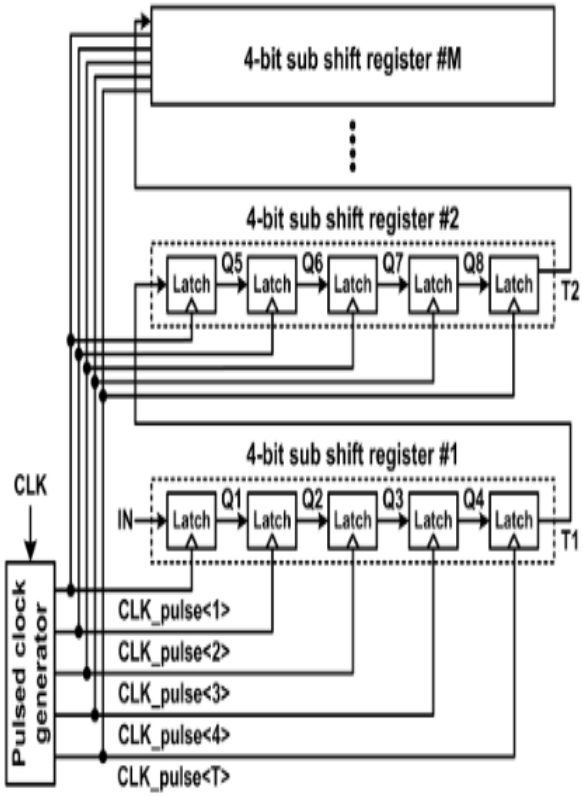
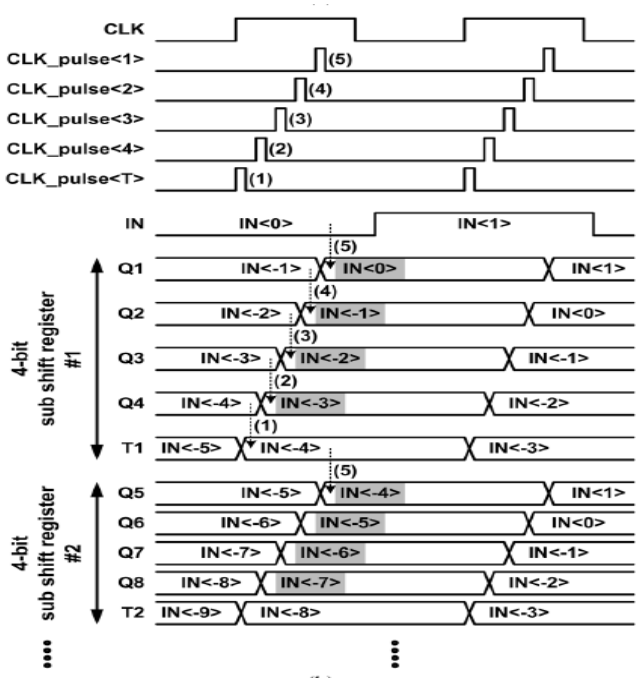


Fig.5. (a) Proposed shift register

Fig. 5. (a) Shows the proposed shift register. The proposed shift register is divided into M sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals (CLK_pulse□1:4□ and CLK_pulse□T□). In the 4-bit sub shift register #1, four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2.



(b) proposed shift register waveforms

Fig.5. (b) Shows the operation waveforms in the proposed shift register. Five non-overlaps delayed pulsed clock signals are generated by the delayed pulsed clock generator. The sequence of the pulsed clock signals is in the opposite order of the five latches. Initially, the pulsed clock signal CLK_pulse□T□ updates the latch data T1 from Q4. And then, the pulsed clock signals CLK_pulse□1:4□ update the four latch data from Q4 to Q1 sequentially.

The latches Q2–Q4 receive data from their previous latches Q1–Q3 but the first latch Q1 receives data from the input of the shift register (IN). The operations of the other sub shift registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register.

The proposed shift register reduces the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches as shown in Fig. 5.

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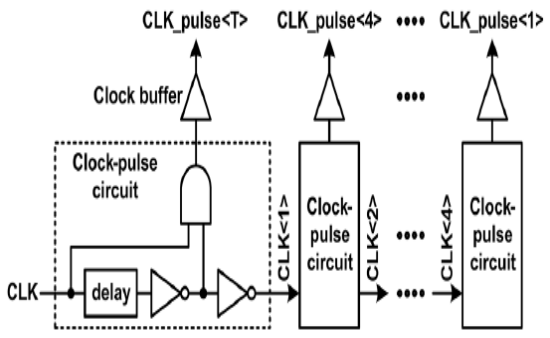

Fig.6. Delayed pulsed clock generator

Each pulsed clock signal is generated in a clock-pulse circuit consisting a delay circuit and an AND gate. When an N-bit shift register is divided into K-bit sub shift registers, the number of clock-pulse circuits is K+1 and the number of latches is N+N/K. A K-bit sub shift register consisting of K+1 latch requires K+1 pulsed clock signals. The number of sub shift registers (M) becomes N/K; each sub shift register has a temporary storage latch. Therefore, N/K latches are added for the temporary storage latches.

The conventional delayed pulsed clock circuits in Fig. 6 can be used to save the AND gates in the delayed pulsed clock generator in Fig. 6. In the conventional delayed pulsed clock circuits, the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuits to keep the shape of the pulsed clock. However, in the delayed pulsed clock generator in Fig. 6 the clock pulsed width can be shorter than the summation of the rising and falling times because each sharp pulsed clock signal is generated from an AND gate and two delayed signals. Therefore, the delayed pulsed clock generator is suitable for short pulsed clock signals.

The numbers of latches and clock-pulse circuit's change according to the word length of the sub shift register (K). K is selected by considering the area, power consumption, speed. The area optimization can be performed as follows. When the circuit areas are normalized with a latch, the areas of a latch and a clock-pulse circuit are 1 and αa, respectively. The total area becomes αa × (K+1) +N (1+1/K). The optimal K (=square root of N/ αa) for the minimum area is obtained from the first-order differential equation of the total area (0=. αa- N/K).An integer K for the minimum area is selected as a divisor of N, which is nearest to (square root of (N/ αa)).

The power optimization is similar to the area optimization. The power is consumed mainly in latches and clock-pulse circuits. Each latch consumes power for data transition and clock loading. When the circuit powers are normalized with a latch, the power consumption of a latch and a clock-pulse circuit are 1 and, respectively. The total power consumption is also "αp × (K+1) + N (1+1/K)". An integer K for the minimum power is selected as a divisor of N, which is nearest to square root of N/ αp. In K selection, the clock buffers in Fig. 3.6. Is not considered. The total size of the clock buffers is determined by the total clock loading of latches. Although the number of latches increases from N to N (1+1/K)". The increment ratio of the clock buffers is small. The number of clock buffers is K.As K increases, the size of a clock buffer decreases in proportion to because the number of latches connected to a clock buffer is k. proportional to 1/K .Therefore, the total size of the clock buffers increases slightly with increasing K and the effect of the clock buffers can be neglected for choosing K.

The maximum number of K is limited to the target clock frequency as shown in Fig. 7 .the minimum clock cycle time is (Tclk_min) is Tcp+K×delay+Tcq, where Tcp is the delay from the rising edge of the main clock signal (CLK) to the rising edge of the first pulsed clock signal (CLK_pulse□T□), is the delay of two neighbor pulsed clock signals, Tcq is the delay from the rising edge of the last pulsed clock signal (CLK_pulse□1□) to the output signal of the latch Q1. Tclk_min is proportional to K.As K increases, the maximum clock frequency (Fclk_min=1/Tclk_min) decreases in proportion to 1/K. Therefore, K must be selected under the maximum number which is determined by the maximum clock frequency of the target applications.

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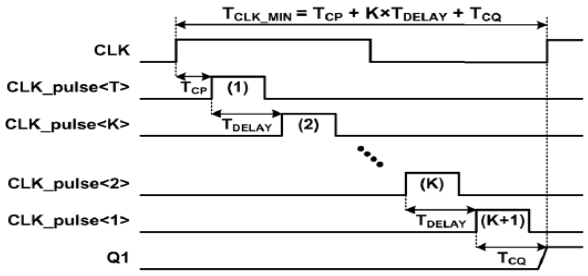

Fig.7. Minimum clock cycle time of the proposed shift register

The K+1 pulsed clock signals in Fig. 7. Are supplied to all sub shift registers. Each pulsed clock signal arrives at the sub shift registers at different time due to the pulse skew in the wire. The pulse skew increases proportional to the wire distance from the delayed pulsed clock generator. All pulsed clock signals have almost the same pulse skews when they arrive at the same sub shift register. Therefore, in the same sub shift register, the pulse skew differences between the pulsed clock signals are very small. The clock pulse intervals larger than the pulse skew differences cancel out the effects of the pulse skew differences. Also, the pulse skew differences between the different sub shift registers do not cause any timing problem, because two latches connecting two sub shift registers use the first and last pulsed clocks (CLK_pulse□ and CLK_pulse□1□) which have a long clock pulse interval.

In a long shift register, a short clock pulse cannot through a long wire due to parasitic capacitance and resistance. At the end of the wire, the clock pulse shape is degraded because the rising and falling times of the clock pulse increase due to the wire delay. A simple solution is to increase the clock pulse width for keeping the clock pulse shape. But this decreases the maximum clock frequency. Another solution is to insert clock buffers and clock trees to send the short clock pulse with a small wire delay. But this increases the area and power overhead. Moreover, the multiple clock pulses make the more overhead for multiple clock buffers and clock trees.

The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there is no delay between flip-flips. Therefore, the area and power consumption are more important than the speed for selecting the flip-flop. The proposed shift register uses latches instead of flip-flops to reduce the area and power consumption. In chip implementation, the SSASPL (static differential sense amp shared pulse latch) in Fig. 8, which is the smallest latch, is selected.

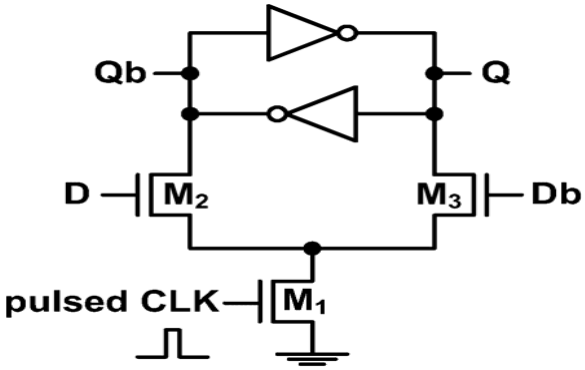

Fig.8.Schematic of the SSASPL

The original SSASPL with 9 transistors is modified to the SSASPL with 7 transistors in Fig. 8 by removing an inverter to generate the complementary data input (Db) from the data input (D). In the proposed shift register, the differential data inputs (D and Db) of the latch come from the differential data outputs (Q and Qb) of the previous latch. The SSASPL uses the smallest number of transistors (7 transistors) and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal.

IMPLEMENTATION

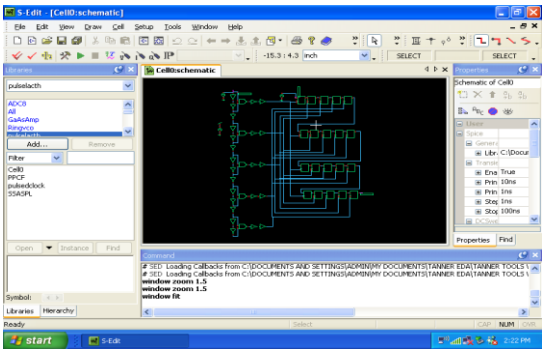

Figure 9: Schematic diagram of proposed system

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The proposed systems of schematic diagram consist of pulsed clock generator and 4-bit sub shift registers. By using pulsed clock generator to share the clock pulse for M-bit sub registers because to reduce the number of delayed pulsed clock signals. In this proposed schematic diagram, the delayed pulsed clock generator uses the two delayed signals, one AND gate and clock buffer. Each row contains 5 latches with clock signals. The main pulsed clock generator shares the clock signals to total latches in the schematic diagram.

SSASPL SCHEMATIC

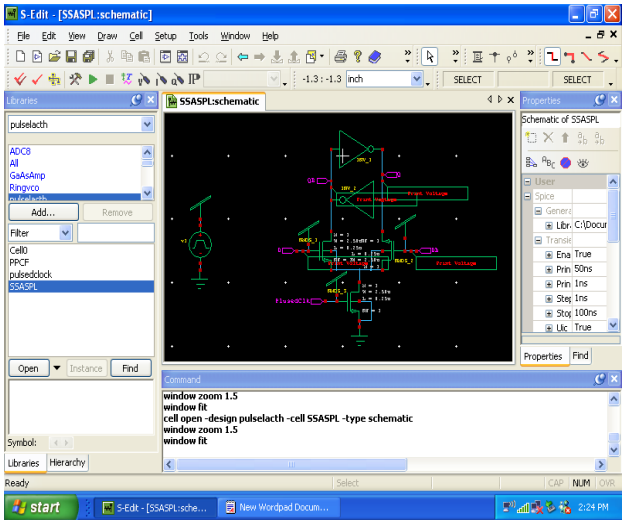

Fig 10: Schematic diagram of SSASPL

The Schematic diagram of SSASPL (static differential sense amp shared pulse latch) consists of three NMOS transistors and two cross-coupled inverters. The three nmos transistors are nmos-1, nmos-2 and nmos-3 and two cross-coupled inverters are inv-1 and inv-2.

It requires two differential data inputs, two differential data outputs and a pulsed clock signal. The name of the two differential data inputs are D and Db and the name of the two differential data outputs are Q and Qb. Db means complementary data input and Qb means complementary data output. The three nmos transistor names are nmos-1, nmos-2 and nmos-3. The voltage signal is given to the three NMOS transistors and the pulsed clock signal is given to the nmos-1 transistor.

PULSED CLOCK SCHEMATIC

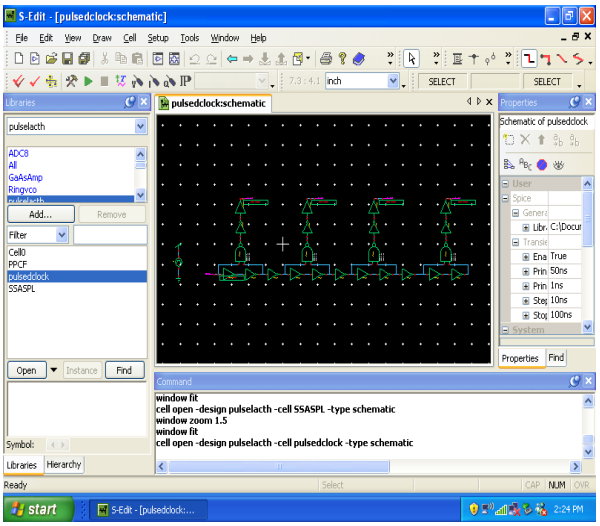

Fig 11: Schematic diagram of the pulsed clock

The schematic diagram of the pulsed clock generator is contains the AND gate and two delayed circuits. The above schematic diagram is formed with the four delayed pulsed clock generators. The proposed system of each latch contain this delayed pulsed clock. The inverters of the delayed pulsed clock gnerator is used to summate the rising tim and falling time of the clock signal. Finally clock buffer is connected to the AND gate. After the completion of the total procedure to form the clock pulse of the proposed system.

CONCLUSIONS & FUTURESCOPE

The proposed low-power and area-efficient shift register using pulsed latches. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. A small number of the pulsed clock signals are used by grouping the latches to several sub shifter registers and using additional temporary storage latches.

In future of the Low-power and Area Efficient Shift Register Using Pulsed Latches is a chance to reduce power somewhat more by doing modifications in the

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project shift register architecture, and also it can be extended to 256 bit now. It can be move in the future.

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