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High-Speed and Energy-Efficient Carry Skip Adder Using Skip Logic

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Abstract

In this paper, we present a carry skip adder (CSKA) structure that has a higher speed yet lower energy consumption compared with the conventional one. The speed enhancement is achieved by applying concatenation and incrementation schemes to improve the efficiency of the conventional CSKA (Conv-CSKA) structure. In addition, instead of utilizing multiplexer logic, the proposed structure makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. The structure may be realized with both fixed stage size and variable stage size styles, wherein the latter further improves the speed and energy parameters of the adder.

Finally, a hybrid variable latency extension of the proposed structure, which lowers the power consumption without considerably impacting the speed, is presented. This extension utilizes a modified parallel structure for increasing the slack time, and hence, enabling further voltage reduction. The proposed structures are assessed by comparing their speed, power, and energy parameters with those of other adders using a 45-nm static CMOS technology for a wide range of supply voltages. In addition, the power–delay product was the lowest among the structures considered in this paper, while its energy–delay product was almost the same as that of the Kogge–Stone parallel prefix adder with considerably smaller area and power consumption. Simulations on the proposed hybrid variable latency CSKA reveal reduction in the power consumption compared with the latest works in this field while having a reasonably high speed.

I. INTRODUCTION

ADDERS are a key building block in arithmetic and logic units (ALUs) [1] and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. There are many works on the subject of optimizing the speed and power of these units, which have been reported in [2]–[9]. Obviously, it is highly desirable to achieve higher speeds at low-power/energy consumptions, which is a challenge for the designers of general purpose processors. Low power arithmetic circuits have become very important in VLSI industry. Due to the rapid growth of portable electronic component, Adder circuit is the main building block in DSP processor.

Adder is the main component of arithmetic unit. A Complex DSP system involves several adders. The Designers are forced with more constraints are high speed , high throughput , small silicon area and low power consumption. Many design styles of adders exist. Although, Ripple carry adders are the small in design structure but its very slower. Most recently, carry-skip adders [1, 2, 3] are used popularly due to their performance of high speed and small size. Generally, in an N-bit carry-skip adder divided into M-bit number of blocks [1, 4], a long-range of carry signal starts at a block Bi, which rippling through some bits in that block, then it skips some blocks, and ends with a block Bj. Carry-look-ahead and carry-select adders are very fast but far larger and consume much more power than ripple or carry-skip adders.

Two of the fastest known addition circuits are the Lynch-Swartzlander's [5] and Kantabutra's [6]hybrid carry look-ahead adders. They are based on the usage

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of a carry tree that produces carries into appropriate bit positions without back propagation. In order to obtain the valid sum bits as soon as possible, in both Lynch-Swartzlander's and Kantabutra's adders the sum bits are computed by means of carry-select blocks, which are able to perform their operations in parallel with the carry-tree Recently, the near-threshold region has been considered as a region that provides a more desirable tradeoff point between delay and power dissipation compared with that of the sub threshold one, because it results in lower delay compared with the sub threshold region and significantly lowers switching and leakage powers compared with the super threshold region.

In addition, near-threshold operation, which uses supply voltage levels near the threshold voltage of transistors [11], suffers considerably less from the process and environmental variations compared with the sub threshold region. The dependence of the power (and performance) on the supply voltage has been the motivation for design of circuits with the feature of dynamic voltage and frequency scaling. In these circuits, to reduce the energy consumption, the system may change the voltage (and frequency) of the circuit based on the workload requirement [12]. For these systems, the circuit should be able to operate under a wide range of supply voltage levels.

Of course, achieving higher speeds at lower supply voltages for the computational blocks, with the adder as one the main components, could be crucial in the design of high-speed, yet energy efficient, processors. In this paper, given the attractive features of the CSKA structure, we have focused on reducing its delay by modifying its implementation based on the static CMOS logic.

The concentration on the static CMOS originates from the desire to have a reliably operating circuit under a wide range of supply voltages in highly scaled technologies [10]. The proposed modification increases the speed considerably while maintaining the low area and power consumption features of the CSKA. In addition, an adjustment of the structure, based on the variable latency technique, which in turn lowers the power consumption without considerably impacting the CSKA speed, is also presented. To the best of our knowledge, no work concentrating on design of CSKAs operating from the super threshold region down to near-threshold region and also, the design of (hybrid) variable latency CSKA structures have been reported in the literature.

II. PRIOR WORK

Modifying CSKAs for Improving Speed

Alioto and Palumbo [19] propose a simple strategy for the design of a single-level CSKA. The method is based on the VSS technique where the near-optimal numbers of the FAs are determined based on the skip time (delay of the multiplexer), and the ripple time (the time required by a carry to ripple through a FA). The goal of this method is to decrease the critical path delay by considering a non integer ratio of the skip time to the ripple time on contrary to most of the previous works, which considered an integer ratio [17], [20]. In all of the works reviewed so far, the focus was on the speed, while the power consumption and area usage of the CSKAs were not considered. Even for the speed, the delay of skip logics, which are based on multiplexers and form a large part of the adder critical path delay [19], has not been reduced.

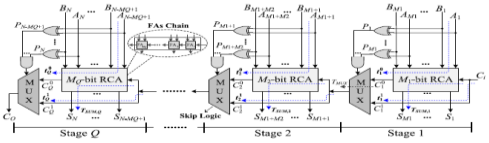

Fig. 1. Conventional structure of the CSKA [19].

Improving Efficiency of Adders at Low Supply Voltages

To improve the performance of the adder structures at low supply voltage levels, some methods have been proposed in. In adaptive clock stretching operation has been suggested. The method is based on the observation that the critical paths in adder units are rarely activated. Therefore, the slack time between the critical paths and the off-critical paths may be used to reduce the supply voltage. Notice that the voltage reduction must not increase the delays of the

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noncritical timing paths to become larger than the period of the clock allowing us to keep the original clock frequency at a reduced supply voltage level. When the critical timing paths in the adder are activated, the structure uses two clock cycles to complete the operation. This way the power consumption reduces considerably at the cost of rather small throughput degradation.

In the efficiency of this method for reducing the power consumption of the RCA structure has been demonstrated. The CSLA structure in [28] was enhanced to use adaptive clock stretching operation where the enhanced structure was called cascade CSLA (C2SLA). Compared with the common CSLA structure, C2SLA uses more and different sizes of RCA blocks. Since the slack time between the critical timing paths and the longest off-critical path was small, the supply voltage scaling, and hence, the power reduction were limited. Finally, using the hybrid structure to improve the effectiveness of the adaptive clock stretching operation has been investigated.

In the proposed hybrid structure, the KSA has been used in the middle part of the C2SLA where this combination leads to the positive slack time increase. However, the C2SLA and its hybrid version are not good candidates for low-power ALUs. This statement originates from the fact that due to the logic duplication in this type of adders, the power consumption and also the PDP are still high even at

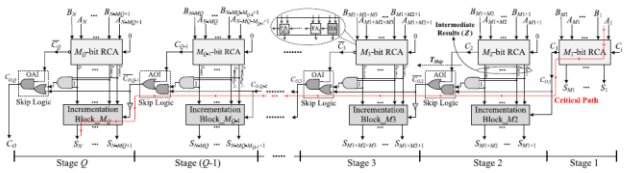

Fig. 2. Proposed CI-CSKA structure.

The reason for using both AOI and OAI compound gates as the skip logics is the inverting functions of these gates in standard cell libraries. This way the need for an inverter gate, which increases the power consumption and delay, is eliminated. As shown in Fig. 2, if an AOI is used as the skip logic, the next skip logic should use OAI gate. In addition, another point to

low supply voltages The CSKA may be implemented using FSS and VSS where the highest speed may be obtained for the VSS structure .Here, the stage size is the same as the RCA block size. In Sections III-A and III-B, these two different implementations of the CSKA adder are described in more detail.

III PROPOSED CSKA STRUCTURE

The structure is based on combining the concatenation and the incrementation schemes [13] with the Conv-CSKA structure, and hence, is denoted by CI-CSKA. It provides us with the ability to use simpler carry skip logics. The logic replaces 2:1 multiplexers by AOI/OAI compound gates (Fig. 2). The gates, which consist of fewer transistors, have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer [37]. Note that, in this structure, as the carry propagates through the skip logics, it becomes complemented. Therefore, at the output of the skip logic of even stages, the complement of the carry is generated. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the conventional one. Note that while the power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the proposed CI-CSKA is a little more than that of the conventional one. This is due to the increase in the number of the gates, which imposes a higher wiring capacitance (in the noncritical paths).

mention is that the use of the proposed skipping structure in the Conv-CSKA structure increases the delay of the critical path considerably. This originates from the fact that, in the Conv-CSKA, the skip logic (AOI or OAI compound gates) is not able to bypass the zero carry input until the zero carry input propagates from the corresponding RCA block.

IV Hybrid Variable Latency CSKA

The proposed hybrid variable latency CSKA uses the RCA blocks along with the parallel prefix adders at some stages. Also here we use variable stage size of

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RCA blocks which leads to the variable latency. Hence the name hybrid variable latency carry skip adder.

In this structure,figure3 there will be only RCA block as the first stage. Remaining stages will have RCA blocks with incrementation blocks.RCA blocks are useful in performing addition and incrementation blocks are useful in getting the final sum.The carry skip logic is useful in determining the carry input for the next stage.In the middle,some stages are modified

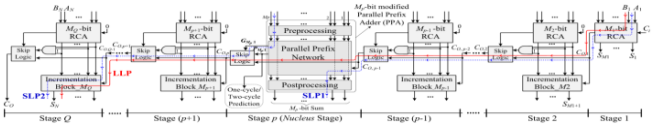

Fig.3.Structure of Hybrid variable latency CSKA

The proposed hybrid variable latency CSKA structure is shown in Fig..3. The predictor block consists of some XOR and AND gates that determines the product of the propagate signals of considered bit positions. Since the block has some area and power overheads, only few middle bits are used to predict the activation of the critical paths at price of prediction accuracy decrease .The basic idea behind using VSS CSKA structures was based on almost balancing the delays of paths such that the delay of the critical path is minimized compared with that of the FSS structure. The prefix adder here used is kogge stone PPA which is specially used for the incresing speed. More over the kogge stone PPA will have larger in layout and minimum fanout for incresing the performance. These PPA are also known as carry look ahead adders.There are also other types of PPAS such as brent kung adder and spanning tree look ahead adder. But as we require incresing speed we will go for kogge stone PPA.

Binary addition is the most fundamental and frequently used arithmetic operation. A lot of work on adder design has been done so far and much architecture has been proposed. When high operation speed is required, tree structures like parallel-prefix adders are used. The Parallel Prefix addition is done in three steps. The fundamental generate and propagate signals are used to generate the carry input for each adder. Two different operators black and gray are used here. The internal by using parallel prefix adders which are called nucleus stage which will have largest size and delay among all the stages. So instead of connecting more number of full adders in RCA block,we can simpy insert only one prefix adder.

By using only one prefix adder instead of chain of fulladders, the wiring will be reduced.Wiring is generally made by using metals.So,if wiring is reduced means the resistance and capacitance will be reduced.
structure of the stage p, including the modified PPA and skip logic, is shown in figure3. Note that, for this figure4.3, the size of the PPA is assumed to be 8 (i.e., Mp = 8). As shown in the figure, in the pre processing level, the propagate signals (P_i) and generate signals (G_i) for the inputs are calculated. In the next level, using kogge stone parallel prefix network, the longest carry (i.e., G8:1) of the prefix network along with P8:1, which is the product of the all propagate signals of the inputs, are calculated sooner than other intermediate signals in this network. After the parallel prefix network, the intermediate carries, which are functions of C_O, P_{-1} and intermediate signals, are computed. Finally, in the post processing level, the output sums of this stage are calculated.

V RESULTS

The design proposed in this paper has been developed using MODEL SIMULATOR. ADDERS are a key building block in arithmetic and logic units (ALUs). Low power arithmetic circuits have become very important in VLSI industry. Adder circuit is the main building block in DSP processor. Adder is the main component of arithmetic unit. A complex DSP system involves several adders. Many design styles of adders exist

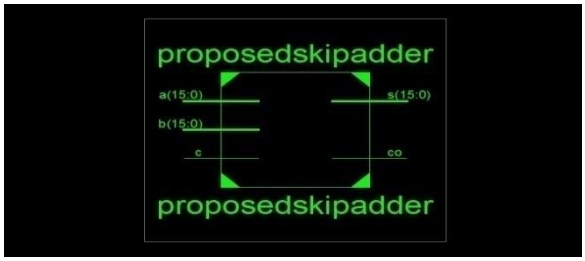

Fig 4Top model RTL Schematic.

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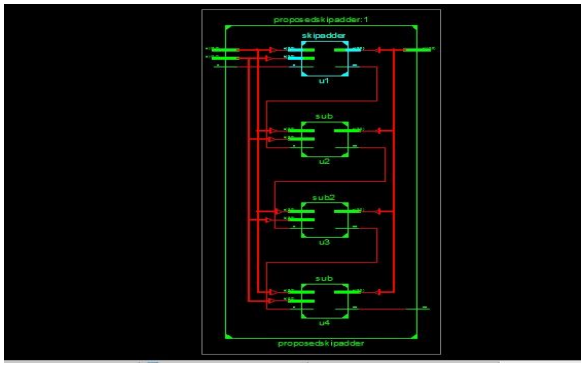

Fig 5 RTL Schematic of CI-CSKA

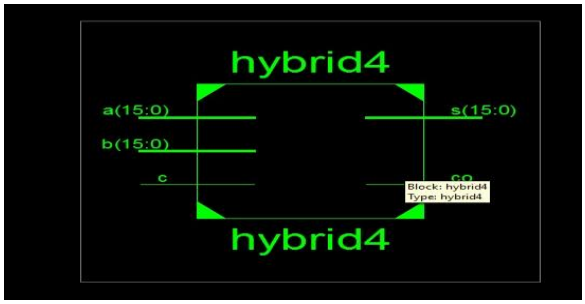

Fig 6Top model RTL Schematic

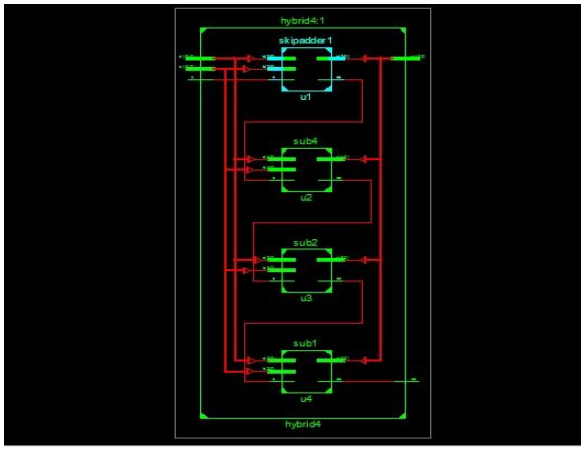

Fig 7 RTL schematic of hybrid variable latency CSKA

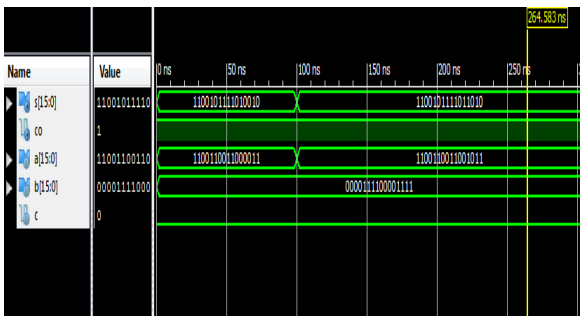

Fig 8 Simulation results

VI. CONCLUSION

In this paper, a static CMOS CSKA structure called CI-CSKA was proposed, which exhibits a higher speed and lower energy consumption compared with those of the conventional one. The speed enhancement was achieved by modifying the structure through the concatenation and incrementation techniques. In addition, AOI and OAI compound gates were exploited for the carry skip logics. The efficiency of the proposed structure for both FSS and VSS was studied by comparing its power and delay with those of the Conv-CSKA, RCA, CIA, SQRT-CSLA, and KSA structures. The results revealed considerably lower PDP for the VSS implementation of the CI-CSKA structure over a wide range of voltage from super-threshold to near threshold. The results also suggested the CI-CSKA structure as a very good adder for the applications where both the speed and energy consumption are critical. In addition, a hybrid variable latency extension of the structure was proposed. It exploited a modified parallel adder structure at the middle stage for increasing the slack time, which provided us with the opportunity for lowering the energy consumption by reducing the supply voltage. The efficacy of this structure was compared versus those of the variable latency RCA, C2SLA, and hybrid C2SLA structures.

Again, the suggested structure showed the lowest delay and PDP making itself as a better candidate for high-speed low-energy applications.

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