ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Design and Analysis of Transient Operation Assessment of RFCLs in Bulk Power Systems

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INTRODUCTION

Demand on electricity has been increasing tremendously and many countries invest significant amount of money for reliable power supply. More generation plants and transmission lines were constructed and the power systems became more complex. Major transmission lines tend to be long-distance and generation sites are large-scaled. Load concentration requires more transmission lines to be interconnected. However, those characteristics of power systems have been causing problems related to fault currents and system stabilities. Several approaches to cope with the fault current problems are being used in distribution and transmission areas.

Permanently-inserted series reactors, up-rating and replacement of switchgear, splitting buses or transmission lines are the most commonly used techniques to limit the fault current in power systems, which are regarded as cost-effective and more secure measures for the operational reliability of power system facilities. However, up-rating and replacement of switchgear can be very expensive and short-circuit current duty may not be reduced. Network splitting can deteriorate the power system security. Permanently-inserted current-limiting series reactors introduce a voltage drop, active and reactive power losses and also adversely affect the power system stability. In spite of these drawbacks, a lot of power systems are still divided into several subsystems to solve fault current problems. For the power system stability enhancement, on the other hand, the following has been used as countermeasures in general: (1) Constructing more interconnection lines, (2) Installing dynamic reactive resources, (3) Constraining power transfers, and (4) Using Special Protection Schemes (SPS).

So far, fault current and stability analysis has been studied separately, since network configuration influences in an opposite way to those problems. When transmission systems are fully meshed, they tend to yield fault current problems, rather than stability problems. On the other hand, when powers are delivered through high impedance transmission lines, stability issues may arise instead of fault current problems. However, as the power systems become more complex with the meshed transmission networks which are interconnected with long-distance, high-power transfer transmission lines, those two problems become co-existent. Consequently, countermeasures to deal with the fault current impact more on the power system stability than before.

The importance of using sustainable sources of energy will have a critical impact on future power systems, and is already leading to an increased presence of distributed generation (DG), microgrids, DC systems, and power electronic devices. These developments add further diversity to electrical sources and loads, and thereby complicate the system protection and control. For future power systems to cater for these fundamental changes, in many cases fault current levels will increase. For example, resiliency against blackouts is of importance in both grid and isolated networks. This, amongst other

Cite this article as: B.Yogananda Reddy, E.Nagabhushana & C.Viswanath, "Design and Analysis of Transient Operation Assessment of RFCLs in Bulk Power Systems", International Journal & Magazine of Engineering, Technology, Management and Research, Volume 5 Issue 9, 2018, Page 115-123.

ISSN No: 2348-4845
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factors, may necessitate increased electrical network inter- connection, which normally increases fault current levels. The connection of DG can also significantly increase fault levels and disrupt protection coordination. Furthermore, the fault current levels in power-dense marine vessel and aircraft power systems are inherently high Safe network operation is very challenging in systems with a high fault level. Power system faults can cause significant damage to life and to equipment at the point of fault and to any equipment carrying fault current. Circuit breakers must be rated to clear faults for a particular system fault current level; higher fault currents lead to higher circuit breaker costs. A key solution to these issues is the adoption of fault current limitation in electrical systems. Fault current limiter (FCL) devices typically do not affect power system operation during normal conditions, yet rapidly act to mitigate the destructive and other undesirable effects caused by power system faults.

FAULT CURRENT LIMITERS

Damage from short circuit currents is a constant threat to any electric power system, since it threatens the integrity of its generators, bus-bars, transformers, switchgears, and transmission and distribution lines. Building on this statement, the FCL is described below.

ROLE OF FAULT CURRENT LIMITER

As mentioned earlier, the role of the FCL is to limit prospective fault current levels to a more manageable level without a significant impact on the distribution system. Consider a simple power system model, as shown in Figure 2.1, consisting of a source with voltage, internal impedance, load, and fault impedance.

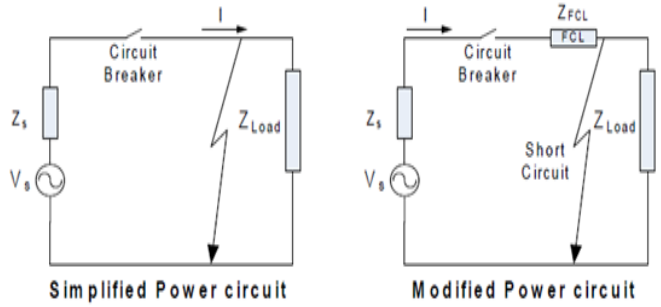

Fig-2.1. Simple power circuit with and without FCL

TYPES OF FAULT CURRENT LIMITERS

This section presents a brief review of the various kinds of FCL that has been implemented or proposed. FCL(s) can generally be categorized into three broad types:

1) Passive limiters
2) Solid state type limiters, and
3) Hybrid limiters

In the past, many approaches to the FCL design have been conducted ranging from the very simple to complex designs. A brief description of each category of limiter is given below. Appendix A of this thesis has a consolidated and more detailed list of the different FCL types.

Passive limiters

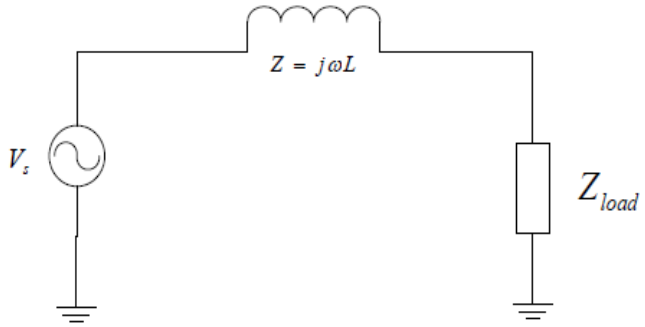

Fig-2.2. Series inductor application as a fault current limiter

Solid-state limiters

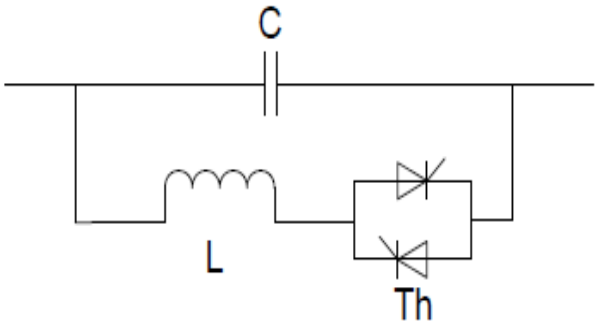

Fig-2.3. Resonant type solid state limiter

Hybrid limiters

As the name implies, hybrid limiters use a combination of mechanical switches, solid state FCL(s), superconducting and other technologies to create current mitigation.

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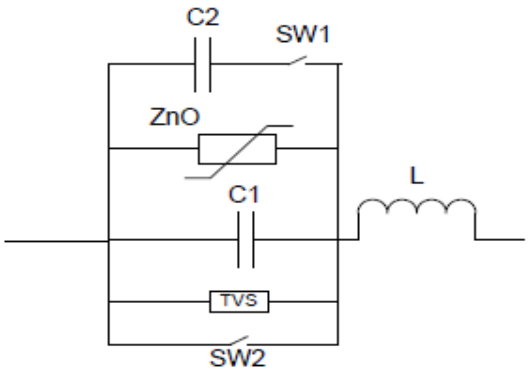

Fig-2.4. Triggered vacuum switch based hybrid limiter

Table 2.1 Comparison of different current limiting approaches

Technologies	Normal losses	Recovery speed	Controlled?	Size	Cost
CL fuses	Low	No recovery	No or Semi-controlled	Small	Low, needs replacement
Mechanical CL breakers	Low	Fast	Yes	Moderate	Moderate to High
Solid-state breakers	Moderate to High	Fast	Yes	Moderate	High
Superconducting FCL (resistive)	Very low	Slow	No	Large	High
Superconducting FCL (assisted)	Very low	Slow	No	Moderate	High
Resonant FCL	Moderate	Fast	Yes	Large	Moderate
Bridge-type FCL	Low to Moderate	Immediate	No or Semi-controlled	Small to Moderate	Moderate
Switched resistance FCL	Moderate	Fast	Yes	Small	Low
Saturated-core FCL	Low	Immediate	No	Large	Moderate

TRADITIONAL MEASURES TO LIMIT FAULT CURRENTS

Current limiting fuses (CLF's)

Current limiting fuses were developed and commercialized as far back as the 1930's, to answer the need for high interruption capacity on low load current rating switchgears. Before the emerging of CLF's, the conventional fuses interrupted a faulted circuit near the first or second current zero. This means that the very first crest of fault current usually the highest peak will be let-through to downstream, leading to possible damage in the apparatus. In response to this issue, an important design principle of any CLF is to develop a reverse voltage high enough to cancel out the system voltage and quickly enough to prevent the first fault current peak from occurring. This characteristic of the CLF effectively limits the fault current (and hence the fault energy, termed as "let-through I2t" in fuse industry) transferred to the downstream device. Also, as a desirable by-product, the operations of CLF's help prevent voltage sags caused by short-circuit faults, which are harmful to computer systems, variable-speed drives, and other industrial systems.

Generally, CLF's have the following characteristics:

a) A transient recovery voltage (TRV) is built up immediately to withstand the system voltage so as to limit the current. In most cases, this TRV is established by creating electric arcs across the melted sections of the fuse elements.

b) CLF's absorb the majority of fault energy, which is stored in the circuit before the elements start to melt.

c) For reactive circuits, overvoltage will present across CLF's when the arc voltages exceed system voltages.

Figure 2.5 is a comparison of typical operation waveform between a conventional expulsion fuse and a CLF. When the fuse melts, the CLF establishes a voltage against the system voltage immediately. When the arc voltage is equal to the system voltage, the fuse current starts to drop from a much lower level than its prospective peak. After this the inductive voltage in the circuit opposes the current drop and adds to the system voltage, developing an overvoltage on the arc inside the CLF. Compared to the traditional expulsion fuse, the CLF has much higher arc voltage, quicker recovery, and much less let-through current or let-through I2t.

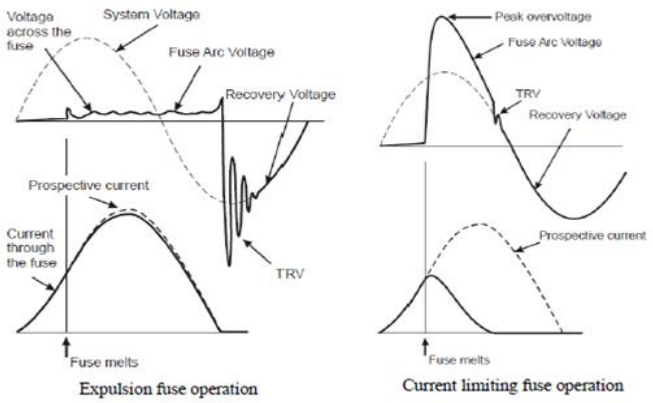

Fig-2.5. Operation waveform of expulsion fuse and current limiting fuse

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STRUCTURE AND OPERATIONAL PRINCIPLE OF A RESONANT FCL

Figure 3.1 illustrates the structure of an RFCL in one of the three phases. The series resonant circuit consists of a current-limiting reactor and a resonant capacitor which are tuned to the rated frequency of the power system to minimize the influence of the RFCL under normal operation. It is not practically possible to perfectly tune a resonant circuit and, thus, little phase shift is unavoidable.

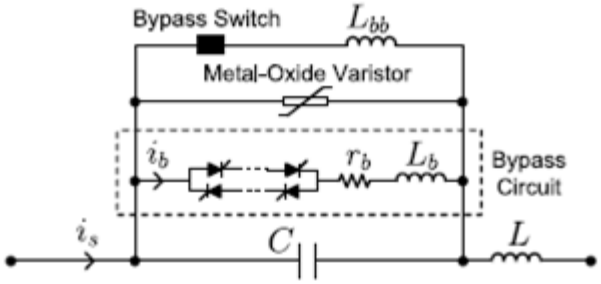

Fig-3.1. Structure of a resonant fault current limiter in one phase.

The figure also depicts that a thyristor-controlled bypass circuit, a metal–oxide varistor, and a bypass switch are in parallel to the capacitor. As soon as a short-circuit fault is detected, the thyristor valves are triggered and the current commutates from the capacitor to the bypass circuit. Therefore, the impedance of the RFCL switches rapidly from almost zero (under normal operation) to the impedance of reactor, which prevents the development of large fault current. The fault is detected by comparing a measure of the line current, where the RFCL is located, with a predefined threshold value. Alternatively, a combination of the current magnitude and its rate of change as well as the duration of their occurrence can be used to detect a fault. The bypass circuit is based on a string of direct light-triggered thyristors in series with a discharge current-limiting reactor and a damping resistor, see Fig. 3.1; these thyristor valves have a high capability during turn-on and the possibility to operate at full potential with a simpler triggering circuit, compared to regular thyristors. The design of the bypass circuit aims to limit the rate of change of discharge current and its peak value after triggering the thyristor valves, and to reduce oscillations of the discharge current during bypass operation. The bypass circuit continues to conduct the current after fault detection.

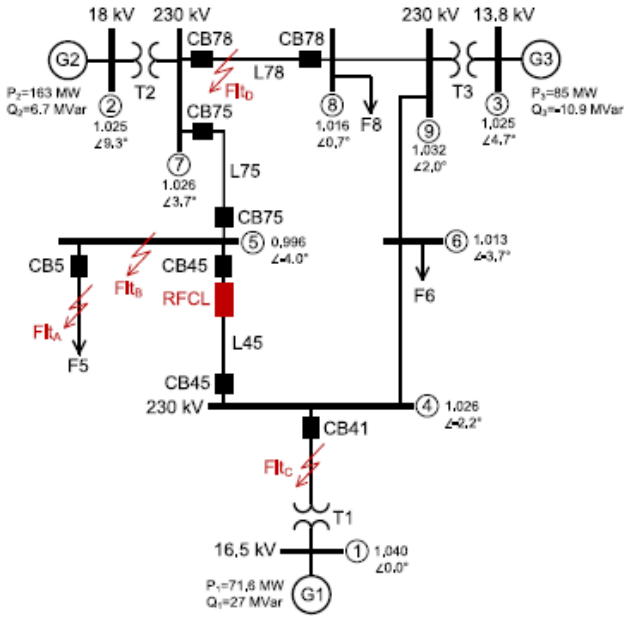

Fig. 2. Nine-bus test power system with an RFCL inserted in line L45.

RFCL DESIGN PROCESS

The process presented in this paper to design the elements of an RFCL and to assess its transient operation in a host power system is a combination of analytical analyses and iterative numerical simulations. Thus, an equivalent network of the overall power system, from where the RFCL is located, which accurately reproduces, during the time period of interest, the same instantaneous values of voltages and currents as those in the overall system can result in a more effective and less timely design process. The bypass circuits in the three phases of the RFCL in Fig.3.2 are triggered as soon as a fault is detected, which occurs within a quarter cycle after the fault strikes the system. Then, the current through line L45 is commutated from the resonant capacitors to the bypass circuits. Therefore, to capture the transient voltage and current stresses in the bypass circuits, in the equivalent network, it should reproduce a steady-state current through line L45,

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similar to that in the overall system, before the inception of the fault, and should also emulate the instantaneous line current for a quarter cycle after the strike of the fault.

Network Reduction

Since the RFCL is located in line L45, the aforementioned line and buses 4 and 5 at its two terminals should be retained in the final equivalent network. Also, to study the faults at feeder F5 and bus 5, it is desirable to retain bus 7 and line L75. The power-flow data can be achieved by solving power-flow equations using power systems simulation tools, such as PSSE. This model is an exact representation of the generators for the prefault steady-state condition and a close approximation for a quarter cycle after the fault strikes, which is the time period of interest required for the RFCL design. Thus, during the aforementioned time period, the state variables of the synchronous generators are assumed to remain unchanged. Moreover, all constant-power loads in the test power system are converted to their equivalent constant-admittance form, whose values are calculated based on the steady-state condition of the system before the strike of the fault. The charging capacitances of the transmission lines are also included in their equivalent models. The network reduction is carried out using the Gaussian elimination method. In this approach, the power system under study is usually divided into internal, boundary, and external systems, where the internal and boundary systems constitute the study system. In the test power system of Fig. 2, buses 4, 5, and 7 belong to the study system and should be retained and, therefore, the rest of the buses, that is, the external system, need to be eliminated to achieve the reduced network. Bus 5 is located inside the study system and buses 4 and 7 are the boundary buses.

Current-Limiting Reactor

To reduce the current through line L45, for faults and below its value in the case without RFCL, the value of the current-limiting reactor can be calculated, using the parameters of the equivalent network and based on the desired amount of reduction in the line current.

Bypass Circuit Design

The thyristor valves in the bypass circuit are triggered when a fault is detected and, thus, the current starts to transfer from the resonant capacitor into the bypass circuit. The current through the bypass circuit includes a discharge current superimposed on the current due to the fault. Therefore, the elements of the bypass circuit should be designed to limit the rate of change of discharge current and its peak instantaneous value below their permitted maximum values, which, in turn, are determined based on the current withstanding ratings of the valves. The maximum rate of change of discharge current occurs when the bypass valves are triggered at the maximum possible instantaneous voltage across a resonant capacitor, which, in turn, is equal to the protection level voltage of the varistor. Moreover, reactor limits the initial rate of change of the discharge current when the valves are triggered.

Energy Absorption Capacity of Varistors

As previously mentioned, the resonant capacitors are not bypassed during the transient time periods subsequent to the strike of faults or and, thus, their parallel varistors are required to protect the capacitors against transient overvoltages by absorbing the extra energy. Moreover, the varistors also protect the resonant capacitors during their insertion in the line, after they had been bypassed in response to the strike of fault. Thus, when fault is cleared by opening breaker CB5, it is desired to insert the capacitor in line L45, in order to compensate reactor and, therefore, to avoid reducing the maximum capacity of line L45 to transfer power. The amount of energy absorbed by a varistor during a transient time period can be calculated by integrating, over time, the product of the current through the varistor and the voltage across its terminals.

This, in turn, can be achieved using the time-domain simulation of the system. In this paper, an ideal volt-ampere characteristic is assumed for the varistors and, therefore, the voltages across the capacitors are not allowed to exceed, while the extra current flows through the varistors.

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SIMULATION RESULTS

To compare the transient responses of the equivalent network with and without the RFCL in line L45, to the nine-bus test system, both networks are simulated in MATLAB/SIMULINK simulation results. In the nine-bus system, dynamic models of the generators, including their exciter and governor models, are utilized, whose parameters are given.

CASE A- BYPASS AND INSERTION OF RESONANT CAPACITORS:

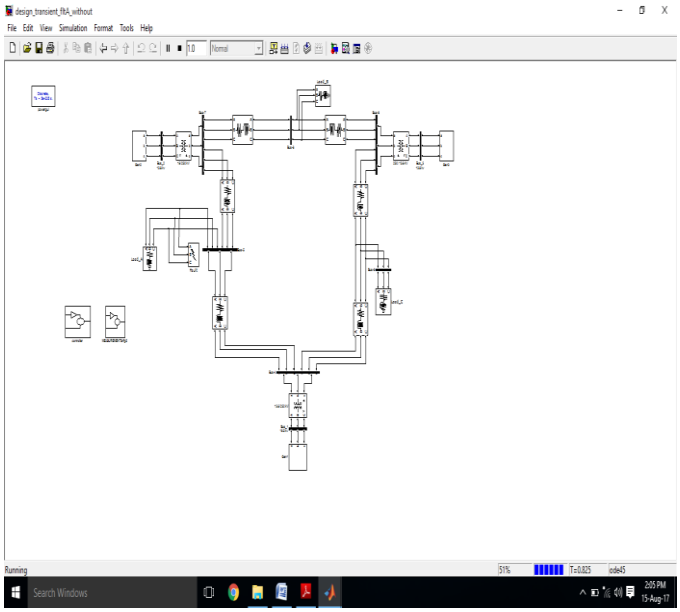

Fig:4.1 Responses of the nine-bus system to the strike of fault FltA without RFCL

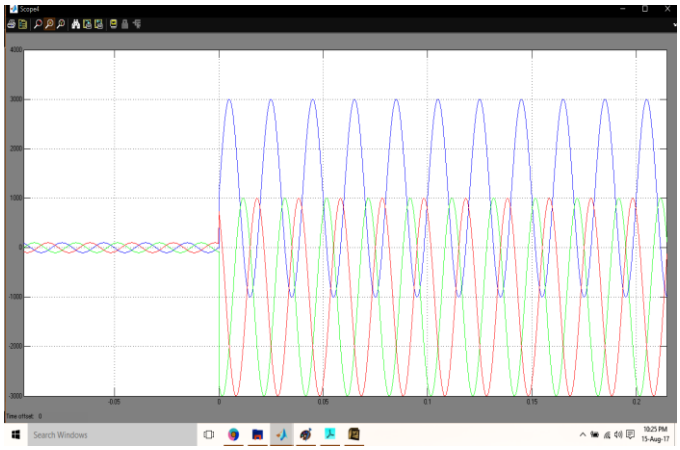

Fig:4.2 Responses of the nine-bus system to the strike of fault FltA without RFCL of a current.

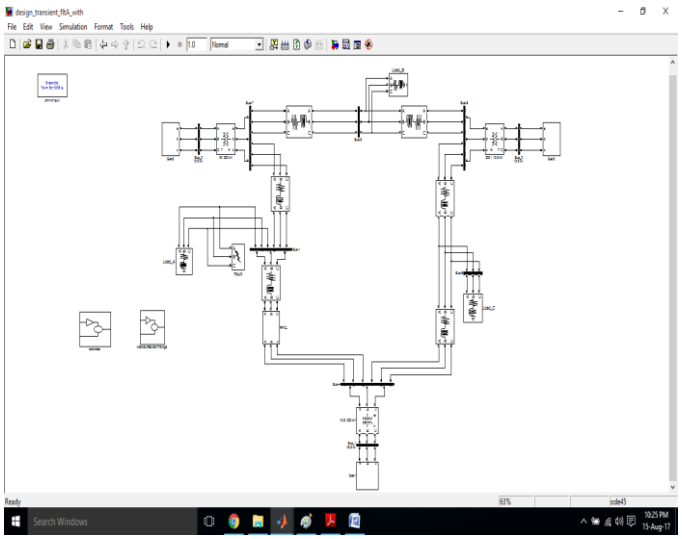

Fig:4.3 Responses of the nine-bus system to the strike of fault FltA with RFCL.

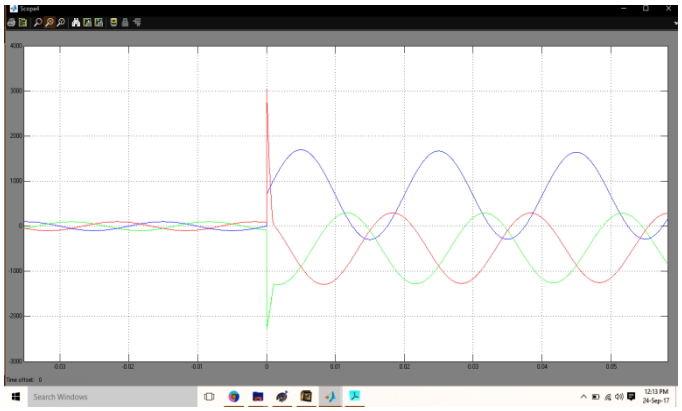

Fig:4.4(a)

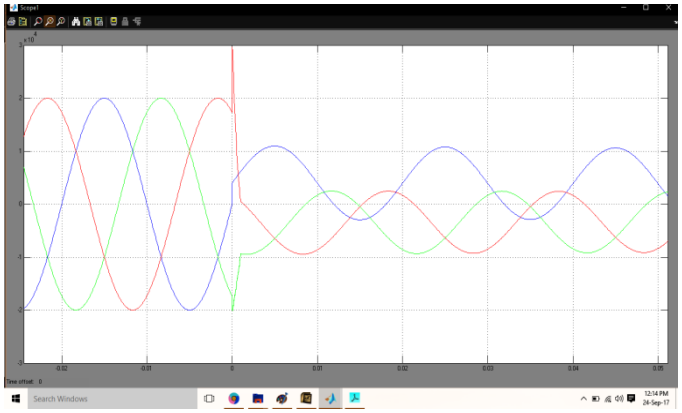

Fig:4.4(b)

Fig:4.4 Responses of the nine-bus system to the strike of fault FltA with RFCL of a current and voltage.

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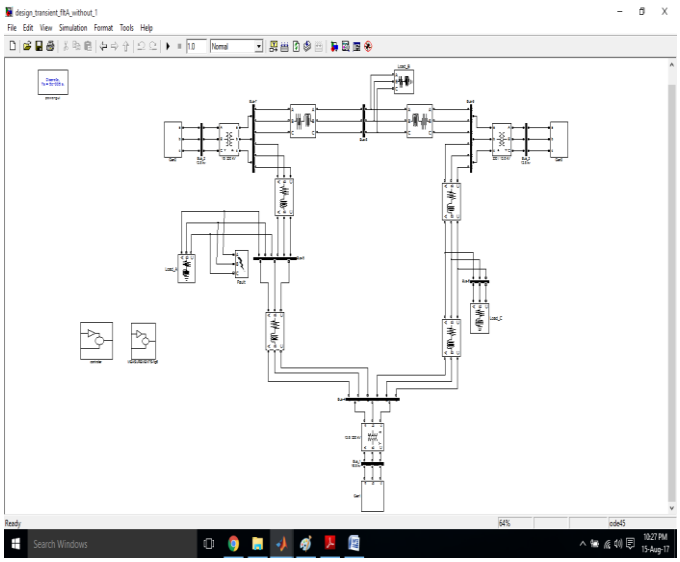

Fig:4.5 Responses of the nine-bus system without RFCL

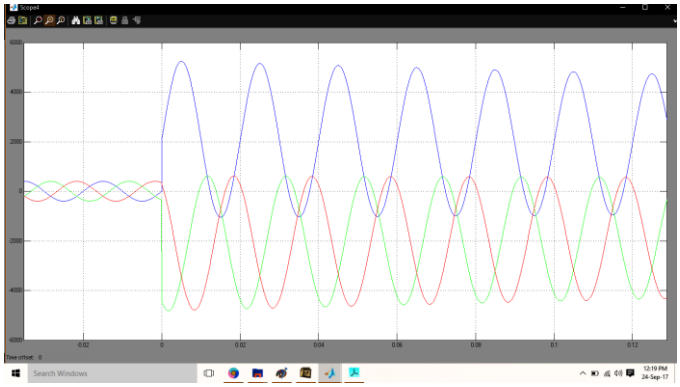

Fig:4.6 Instantaneous currents through breaker CB5 in the nine-bus system without RFCL in line L45.

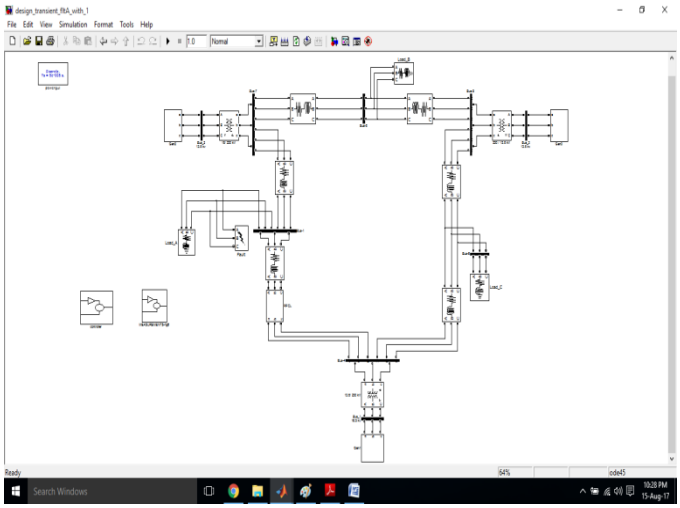

Fig:4.7 Responses of the nine-bus system without RFCL

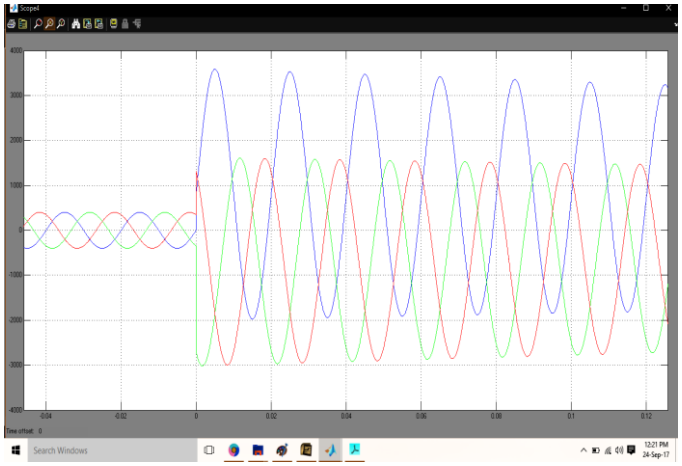

Fig:4.8 Instantaneous currents through breaker CB5 in the nine-bus system with RFCL in line L45.

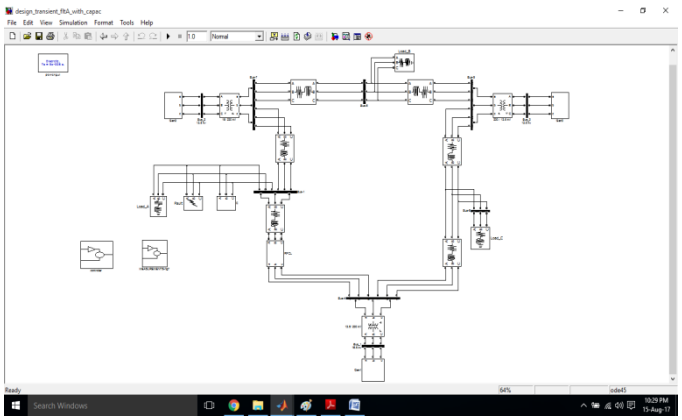

Fig:4.9 Responses of the nine-bus system to the capacitor insertion after the clearance of fault FltA.

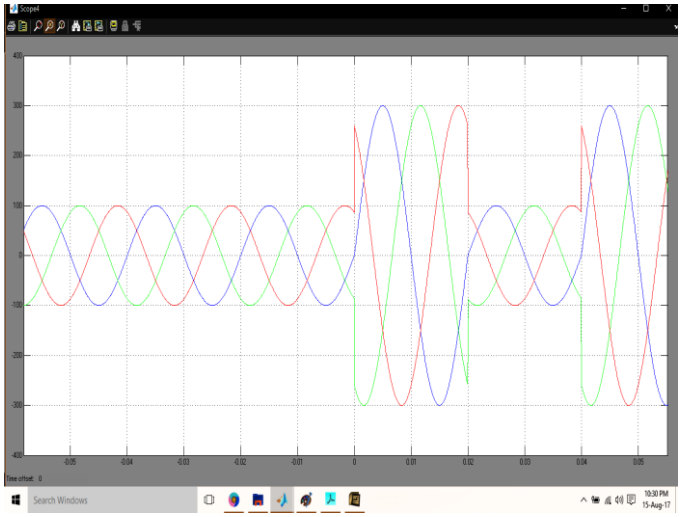

Fig:4.10(a)

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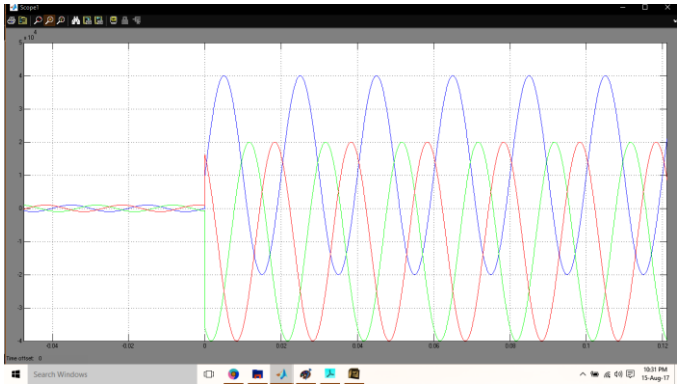

Fig:4.10(b) Responses of the nine-bus system to the capacitor insertion after the clearance of fault FltA. (a) Line currents. (b) Capacitor voltages.

It is observed that subsequent to the fault initially, the voltages across the capacitors increase due to the rise in the line current. Then, after the bypass valves are triggered, the line current commutates to the bypass circuit and the voltages across the capacitors drop. Fig. 4.2 & 4.4 plots the responses of the nine-bus test system in the two cases of without RFCL and with an RFCL in line L45, where at 0 s, fault strikes the system in each case.

In the case of the RFCL, the protection-level voltage of the varistors is selected equal to two times the capacitor voltage under normal operation, that is, 43 kV, and the current threshold is equal to four times the current through line L45 under normal operation, that is, 800 A. It is observed that the responses of the nine-bus system and its equivalent network, in the two cases, are in close agreement during the prefault and a quarter cycles after the inception of the fault.

Fig. 4.6 & 4.8 also plots the instantaneous currents through breaker CB5 in the nine-bus system in the two cases of without RFCL and with the RFCL in line L45. It is observed that the peak value of the current is reduced from 5 kA to 3.5 kA, that is, 30% reduction. Fig. 4.10 illustrates the responses of the nine-bus system when the resonant capacitors are inserted in line L45 after the clearance of fault, under the assumption that the system is at steady state before 0 s. Thus, Fig. 4.10 depicts that the responses of the nine-bus system and its equivalent network are generally in agreement despite the discrepancies. Since the capacitor voltages remain below, no energy is absorbed by the varistors.

CONCLUSION

This project presented a comprehensive framework to design RFCLs in bulk power systems. The elements of an RFCL were initially designed based on a combination of mathematical analyses and numerical time-domain simulations, using an equivalent network of the test power system which reproduces the instantaneous currents and voltages of the system during the time period of interest. The transient operation of the designed RFCL was then evaluated using the time-domain dynamic model of the overall test system. Finally, the framework was used in a real transmission system to design RFCLs inserted in two interconnecting lines and to assess the impact of their incorporation in the host system. It was concluded that RFCLs are effective devices for reducing the currents due to faults in bulk power systems.

FUTURE SCOPE

A power control strategy based on synchronous frame proportional−integral (PI) regulators with structural simplicity and fast dynamic response is designed to control the proposed current source inverter (CSI) based module-integrated converter (MIC) system. The three-phase PV MIC system, it would be required for MIC to be equipped with the real-time active and reactive power control capability to fulfill the upcoming grid requirements. Such as analyzing stability of the closed-loop control systems and coordinating the output power of the high number of the CSI-based MIC units as large-scale grid-tied PV systems. Different faults of the system should can be studied, and correspondingly proper protection and control systems can be designed for the CSI.

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ISSN No: 2348-4845
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